EK-TSV05-UG-001

TSV05
Tape Transport Subsystem

User's Guide

digital

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User's Guide

Prepared by Computer Special Systems
of
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CHAPTER 1
INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual describes how to unpack, install, and check out the TSVØ5 Tape Transport Subsystem. It also describes the capabilities and basic functions of the subsystem. An overview of the functional characteristics and the physical specifications appears in Chapter 1, while Chapter 2 is devoted to the installation. Chapter 3 discusses various aspects of system operation, including routine operating procedures and programming requirements. For further information, refer to the documents listed in Section 1.4.

1.2 GENERAL DESCRIPTION

The TSVØ5 Tape Transport Subsystem provides magnetic tape storage capabilities to computer systems using quad-sized LSI-11 bus backplanes. The subsystem reads or writes up to 160,ØØØ bytes per second in ANSI standard format. Data is recorded by phase encoding 16ØØ bits per inch on nine-track tape. Reading and writing are performed at either 25 or 1ØØ inches per second.* The TSVØ5 subsystem is hardware compatible with 18- and 22-bit addressing versions of the LSI-11 bus quad backplane. It is software compatible with system and application programs written for the TS11 tape transport subsystem (as long as such programs use the DEC-supplied device handler). Tape formatting, error detection and correction, and self-test diagnostics are included as integral components of the TSVØ5 subsystem.

The TSVØ5 hardware consists of four items:

1. TSØ5 tape transport
2. M7196 LSI-11 bus interface/controller module
3. H9642-series cabinet, including 874 power controller and remote power control cable
4. Pair of 7Ø16855 bus cables for connecting tape transport input and output to the bus interface/controller module.

The bus interface/controller module plugs into the LSI-11 bus (see Figure 1-1). The two cables connect the module with the tape transport.

*1ØØ IPS operating speed requires enabling special features and the appropriate software.

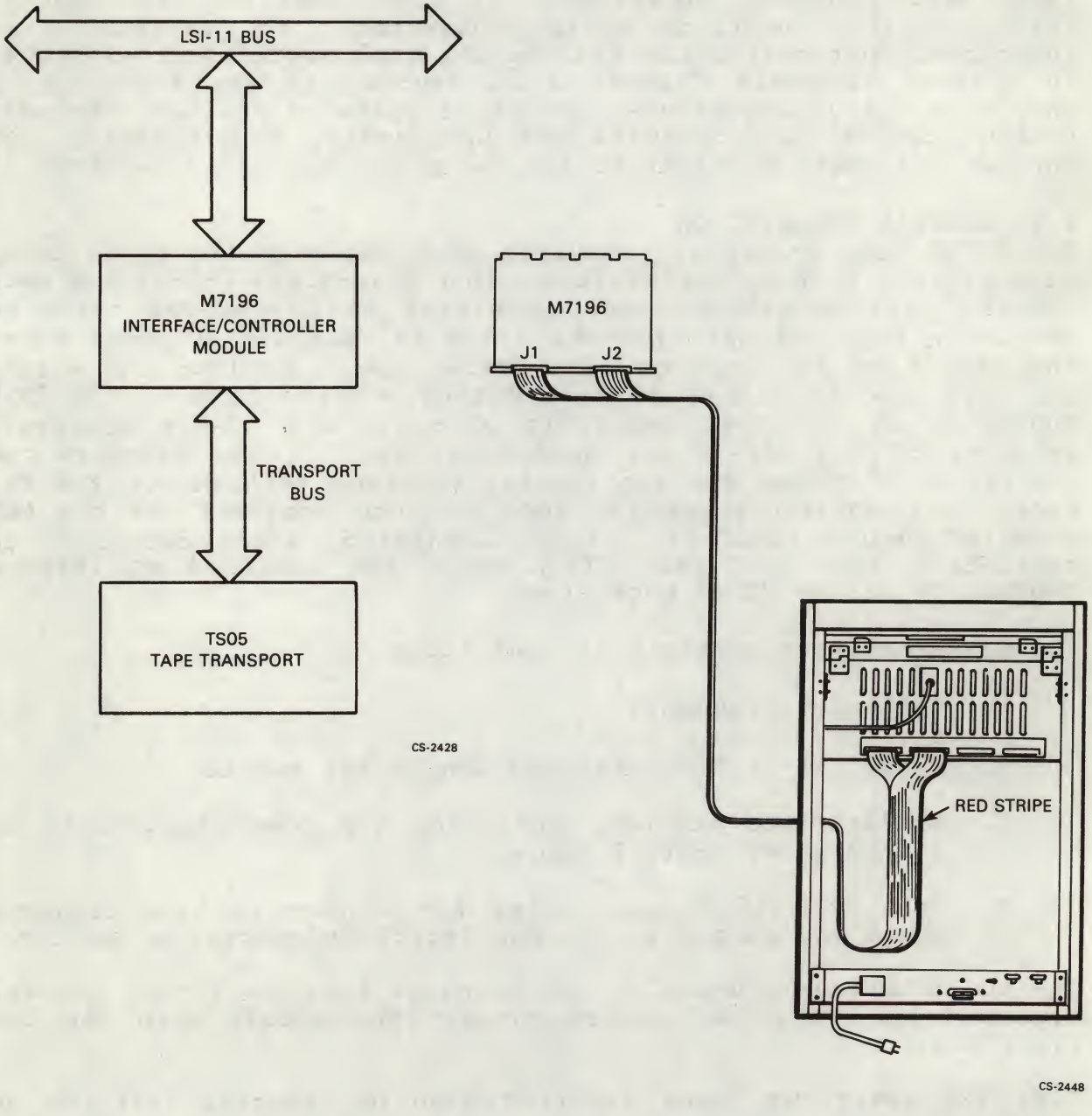


Figure 1-1 TSV05 Subsystem Components

1.2.1 Features and Capabilities

The TSV05 Tape Transport Subsystem offers the following:

- Bidirectional reading capability
- 3.5K bytes of RAM in controller for buffering tape data
- Streaming, or reel-to-reel, technology (meaning that the tape is not required to stop in the interrecord gap)
- Automatic tape loading (threading)
- Microprocessor control in both the controller and the tape transport
- Microcoded diagnostic and maintenance features
- Tape formatting and error detection following ANSI X 3.39-1973 Standard
- Both ANSI and IBM tape mark detection
- Industry standard bus between controller and tape transport
- On-line diagnostics that verify data path integrity during idle periods
- Uses media conforming to ANSI X 3.40-1976 Standard
- Automatic read after write verification
- Small form factor with low power consumptions.

The tape handling characteristics and parameters are as follows:

Tape Characteristics

Type:	Mylar base, iron-oxide coated
Length:	731 m (2400 ft) maximum
Width:	1.3 cm (0.5 in)
Thickness:	1.5 mil (industry compatible)
Reel Diameter:	26.7 cm (10.5 in) 2400 ft 21.6 cm (8.5 in) 1200 ft 17.8 cm (7.0 in) 600 ft
Capacity/Tape Reel:	46 million bytes (10.5 in reel, unformatted)

Tape Motion

Handling:	Bidirectional reel-to-reel, with compliance arm
Tape Tension:	212.6 g (7.5 oz) nominal
Read/Write Speed:	64 cm/sec (25 in/sec) (using TS11 software)
	64 or 254 cm/sec (25 or 100 in/sec) (program selectable using special software)
Rewind Speed:	330 to 457 cm/sec (130 to 180 in/sec) (nominal), depending on reel size
	445 cm/sec (175 in/sec) (average), using 26.7 cm (10.5 in) reel

Rewind Time:

Reel Size, cm (in)	Minutes, maximum
17.8 (7.0)	0.9
21.6 (8.5)	1.6
26.7 (10.5)	2.8

Auto Loading

Reliability:	An average of 96% of attempted loads will be successful, with automatic retries, assuming a properly maintained transport and tape library.
Retries:	Three automatically provided.
Times:	30 sec typical with no retry 30 sec maximum for each additional retry

Unloading

Time:	15 sec maximum with tape located at BOT

Tape Speed Variation:

Long Term:	± 1% of nominal
Instantaneous:	± 4% of long term

Data Access Times:

	64 cm/sec (25 in/sec)	254 cm/sec (100 in/sec)
Tape at Rest:	40 ms	260 ms
Worst Case:	140 ms	1040 ms

Data Transfer Rate:	40K bytes/sec at 64 cm/sec (25 in/sec)
	160K bytes/sec at 254 cm/sec (100 in/sec)

Data Organization

Number of Tracks:	Nine (eight data; one parity)
Recording Density:	1600 bits/in (nonselectable)
Interrecord Gap:	1.3 cm (0.5 in) minimum, 1.65 cm (0.65 in) typical at 64 cm/sec (25 in/sec)
Recording Method:	Phase encoded (PE)
Error Rates:	Recoverable Write: 1 error in 10^8 bits transferred
	Recoverable Read: 1 error in 10^9 bits transferred
	Unrecoverable Read: 1 error in 10^{10} bits transferred

The LSI-11 bus interface characteristics are as follows:

Address Space Required:	772520/772522	1st	unit
	772524/772526	2nd	unit
	772530/772532	3rd	unit
	772534/772536	4th	unit
Vectors Required:	224	1st	unit
	*	2nd	unit
	*	3rd	unit
	*	4th	unit

1.2.2 Functional Overview

Tape loading is automatic. There are no vacuum columns, retaining clips, or multiple tension arms. When the tape transport is powered up, sets of internal diagnostics are run by the microprocessors in the tape transport electronics package and the bus interface/controller module. The subsystem is then ready for loading. Once the tape has been inserted and the door closed, the TS05 tape transport automatically seats and locks the tape reel on the spindle, and threads the tape through the correct path to the takeup reel. The threading operation is accomplished by precisely directed air flows that blow the tape along the path to the takeup reel. When this power up and load sequence is complete, control of the tape transport switches to the controller module.

*Rank of 37 in the floating vector area starting at 300.

The TSVØ5 subsystem operates under the control of a microprocessor on the M7196 bus interface/controller module. The module is a direct memory access (DMA) device in that it transfers data directly into or out of the LSI-11 memory without requiring the control of the LSI-11 CPU. To perform a data transaction with the TSVØ5 subsystem, the LSI-11 first builds a "packet" of command words in main memory. Next, it passes the starting address of the command packet to the M7196 module. Using this address, the M7196 module performs a DMA transfer to bring the command packet out to the controller memory. The command packet tells the controller what type of operation is to be performed and where the data is to come from or go to. The module then controls the movement of data from LSI-11 memory to the tape, or from tape to memory. It buffers this data so that DMA transfers can be handled independently of the mechanical movements of the tape. Additionally, it generates interrupts when necessary to provide the LSI-11 with status information.

The TSØ5 tape transport has an internal formatter that controls tape motion, formatting and writing of data on tape, reading of data from tape, and tape transport status monitoring. Commands from the M7196 module are latched into registers and then processed by a microprocessor in the formatter electronics. The formatter creates the identification (ID) burst, preamble, post amble, and file mark during a write operation, and it interprets these during a read operation. The formatter also oversees the handling of error conditions.

1.2.3 Controls and Indicators

The M7196 bus interface/controller module has jumpers, DIP switchpacks, and LED indicators. The jumpers and switchpacks are preset to the normal configuration and do not need to be changed unless there is an address conflict with an existing device. The LED indicators are provided as maintainability features, and are not exposed to view during normal operation.

The TSØ5 tape transport has an ON/OFF (1/Ø) power switch and five tactile switches, each with an LED indicator. (Refer to Figure 1-2.) The functions of these controls and indicators are described in Table 1-1. The TSØ5 tape transport also has internal switches for selecting tape units and enabling certain features, but these are preset and normally not changed. It also has an LED fault indicator. This LED is not exposed to view during normal operation.

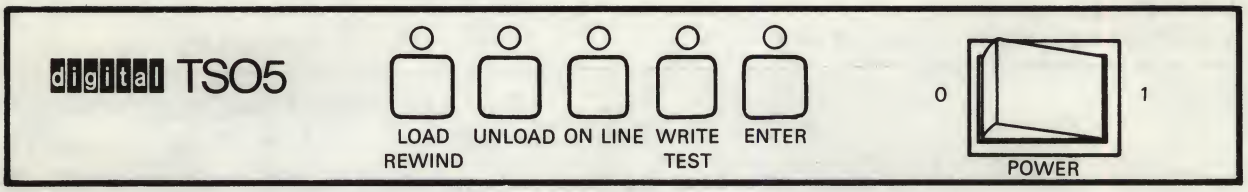


Figure 1-2 Operator Front Panel

Table 1-1 Controls and Indicators

Control/ Indicator	Type	Function
POWER	On/off rocker switch and indicator	Switches line power on and off.
LOAD REWIND	Tactile switch and indicator	1. Blinks when the tape drive is executing a load or rewind sequence. 2. Lit continuously when the beginning of tape (BOT) marker is sensed. 3. Pressing the switch: a. Initiates load sequence and advances tape to load point. b. Rewinds the tape to load point.
UNLOAD	Tactile switch and indicator	1. Pressing the switch causes the tape to be unloaded regardless of tape position. 2. Blinks when the tape drive is executing an unload sequence.

Table 1-1 Controls and Indicators (Cont)

Control/ Indicator	Type	Function
		3. Lit continuously when the tape drive has completed its unload sequence and the front access door is unlocked. At this time, the tape may be removed and another tape inserted into the drive. 4. Lit continuously after a successful power up, indicating a tape may be loaded.
ON-LINE	Tactile switch and Indicator	1. Lit when drive is ready and on-line. 2. Pressing the switch: a. Takes the tape drive off-line and extinguishes the indicator. b. Puts the tape drive on-line and lights the indicators. NOTE Pressing the switch during a load sequence puts the tape drive on-line when the BOT marker is sensed.
TEST	Tactile switch	Operational only in the test mode. Selects alternative operational mode for other switches.
WRITE	Indicator	1. Lit when the write ring is installed and data may be written on tape. 2. When indicator is off, write ring is not installed and tape is file protected.
ENTER	Tactile switch	This control is used for manual loading, and controlling the test mode.

1.3 PHYSICAL DESCRIPTION

1.3.1 Mechanical Characteristics

Tape Transport Cabinet

Height: 111.13 cm (43.75 in)

Width: 59.69 cm (23.50 in)

Depth: 83.82 cm (33.00 in)

Weight: 121 kg (265 lb)

M7196 Bus Interface/Controller Module

Length: (From contact fingers to handles): 228.6 mm (9.0 in)

Width: 266.7 mm (10.5 in)

Thickness: 12.7 mm (0.5 in)

Weight: 0.51 kg (1.13 lb)

Formatter Bus Cables

Connectors: 50-pin, right-angle, flat cable header connectors at controller end; industry standard formatter connectors at tape transport end.

Length: 2.4 m (8.0 ft)

1.3.2 Electrical Requirements

Tape Transport Cabinet

Power Consumption: 220 W average
270 W maximum

Voltage (+7% or -15%):

	Nominal, Vdc	Low Limit, Vdc	High Limit, Vdc
TSV05-BA	120	102	128
TSV05-BB	240	204	256
TSV05-BD	220	187	235

Frequency: ± 1 Hz

Nominal, Hz	Low Limit, Hz	High Limit, Hz
50 or 60	49	61

Frequency Rate of Change: 1.5 Hz/sec maximum

M7196 Controller

Power Consumption: 5 Vdc ± 5% at 6.5 A (maximum)

LSI-11 Bus Loading: DC: One load
AC: Three loads (maximum)

1.3.3 Environmental Considerations

1.3.3.1 Operating Conditions -- The TSV05 subsystem is designed to operate under the following conditions:

Temperature

15°C to 32°C

Temperature Shock: 20° C change/hr maximum

Relative Humidity

20% to 80% noncondensing

Altitude

Sea level to 3 km (10,000 ft)

Vibration

Frequency Range: 5 to 500 Hz

Peak Acceleration: 0.25 g, 22 to 500 Hz, 0.01 in DA5-22 Hz

Application: Each of three orthogonal axes

Shock

+10 g peak, Halfsine, 10 ms

Pollutants

Atmospheric Particulates: 60 mg/1000 cu ft air by weight of particle (5 micron diameter)

Electrostatic Discharge

10 kV through 100 ohms from 350 pF

1.3.3.2 **Nonoperating Conditions** -- The TSV05 subsystem is designed to withstand the following conditions during nonoperating periods (e.g., shipping):

Temperature

-40° C to 66° C

Relative Humidity

95% maximum, noncondensing

Altitude

Sea level to 15 km (49,000 ft)

NOTE
Magtape media typically has more restricting nonoperating environmental considerations.

Vibration (in shipping container)

Frequency Range:	10 to 300 Hz
Peak Acceleration:	1.4 g rms vertical axis
	0.68 g rms longitudinal and lateral axis
	200 Hz maximum

Shock (in shipping container)

Peak Acceleration:	20 g
Duration:	30 $\pm$ 10 ms
Waveshape:	1/2 sine

1.3.3.3 **Emissions** -- During normal operation, the TSV05 subsystem is designed to emit no more than the following levels:

Heat

1100 Btu/hr maximum

Acoustic Noise

Standby (blower on):	57 dB A scale
Operating Conditions:	60 dB A scale

Electromagnetic Interference (EMI)

Complies with FCC Part 15, Subpart J, Class A.

Designed to comply with VDE 0871 B requirements.

NOTE

The TSV05 subsystem has been designed and tested to meet Digital standards including FCC requirements. The specifications in this chapter are based on this testing. Digital cannot guarantee the TSV05 subsystem will meet these specifications if nontested equipment is installed into the TSV05 cabinet or the TSV05 cabinet is installed in nontested configurations.

1.4 RELATED DOCUMENTS

Title	Order Number
TSV05 Tape Transport Pocket Service Guide	EK-TSV05-PS
Operation and Maintenance Instructions for Model F880 Tape Transport	799816-000*
TSV05 Tape Transport Subsystem Installation Guide	EK-TSV05-IN
XXDP User Guide	AC-90931-MC
DEC/X11 User Document	AC-8240Z-MC
TS05 Tape Transport Operation and Acceptance Preventive Maintanance Remove/Replace	EY-D3142-PS
TSV05 Field Print Set	MP-01157
TSV05 Subsystem Technical Manual	EK-TSV05-TM
Microcomputers and Memories	EB-18451-20
Microcomputer Interfaces Handbook	EB-17723-20

CAUTION

Reference the appropriate TSV05 Manual for installation, operation, and maintenance information.

*Available from Cipher Data Products, 10225 Willow Creek Road, San Diego, California 92131. This document contains detailed drawings of the TS05 formatter and power supply.

CHAPTER 2
INSTALLATION

This chapter explains the TSV05 Tape Transport Subsystem installation. A section is devoted to each of the following:

1. Site preparation
2. Unpacking and inspection
3. Installing the tape transport cabinet
4. Checking out the tape transport
5. Installing the bus interface/controller module
6. Installing the interconnecting cables
7. Checking out the TSV05 subsystem.

> **NOTE**
>
> BEFORE YOU UNPACK the cartons, inspect for signs of shipping damage. If the shipment has been damaged, call the dealer from whom the equipment was purchased. If the equipment is covered under "Digital Transit Insurance", the Digital representative will estimate the damage and put in a claim. If the equipment is not insured by "Digital Transit Insurance" contact the carrier who handled the equipment and your own insurance company. Digital Field Service is available on a per-call basis to make estimates of damage for any resulting insurance claims.

2.1 SITE PREPARATION

The TSV05 Tape Transport Subsystem mounts to the left side of the existing computer cabinet. It requires a 59.7 centimeter (23.5 inch) wide by 83.8 centimeter (33.0 inch) deep area of floor space that is capable of supporting, as a minimum, 121 kilograms (265 pounds). The cabinet is capable of supporting up to 205 kilograms (450 pounds).

Beyond this mounting space, the TSV05 subsystem also requires room for access to the cabinet, the correct power receptable, and an adequate flow of cooling air.

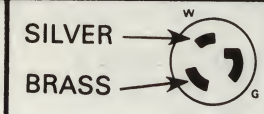
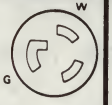
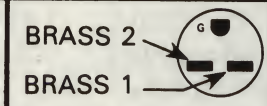
2.1.1 Accessibility

The cabinet requires sufficient space behind it for opening the rear door. If any expansion is anticipated, room in front of the cabinet will be required to allow future equipment to be pulled out of the cabinet for maintenance. Refer to Figure 2-1 for the required dimensions.

2.1.2 Power Receptacles

Ensure that the correct power receptacle is available (refer to Table 2-1). It should be capable of handling at least the 270 watts required by the tape transport.

Table 2-1 Power Line Connections

MODEL	PLUG	RECEPTACLE	CIRCUIT RATING
TSV05-BA	 NEMA #L5-30P DEC #12-11193	 L5-30R 12-11194	120 V 24 A
TSV05-BB -BD	 NEMA #6-15P DEC #90-08853	 6-15R 12-11204	220/240 V 12A

CS-2431

Power Cord Color Code

		Pin Connection	
Color	Function	L5-30P	6-15P
Brown	Hot	Brass	Brass 1
Blue	Neutral	Silver	Brass 2
Green/yellow	Ground	Ground	Ground

2.1.3 Cooling

The TSV05 subsystem requires 1100 Btu per hour of cooling to be provided by the movement of room air through the cabinet.

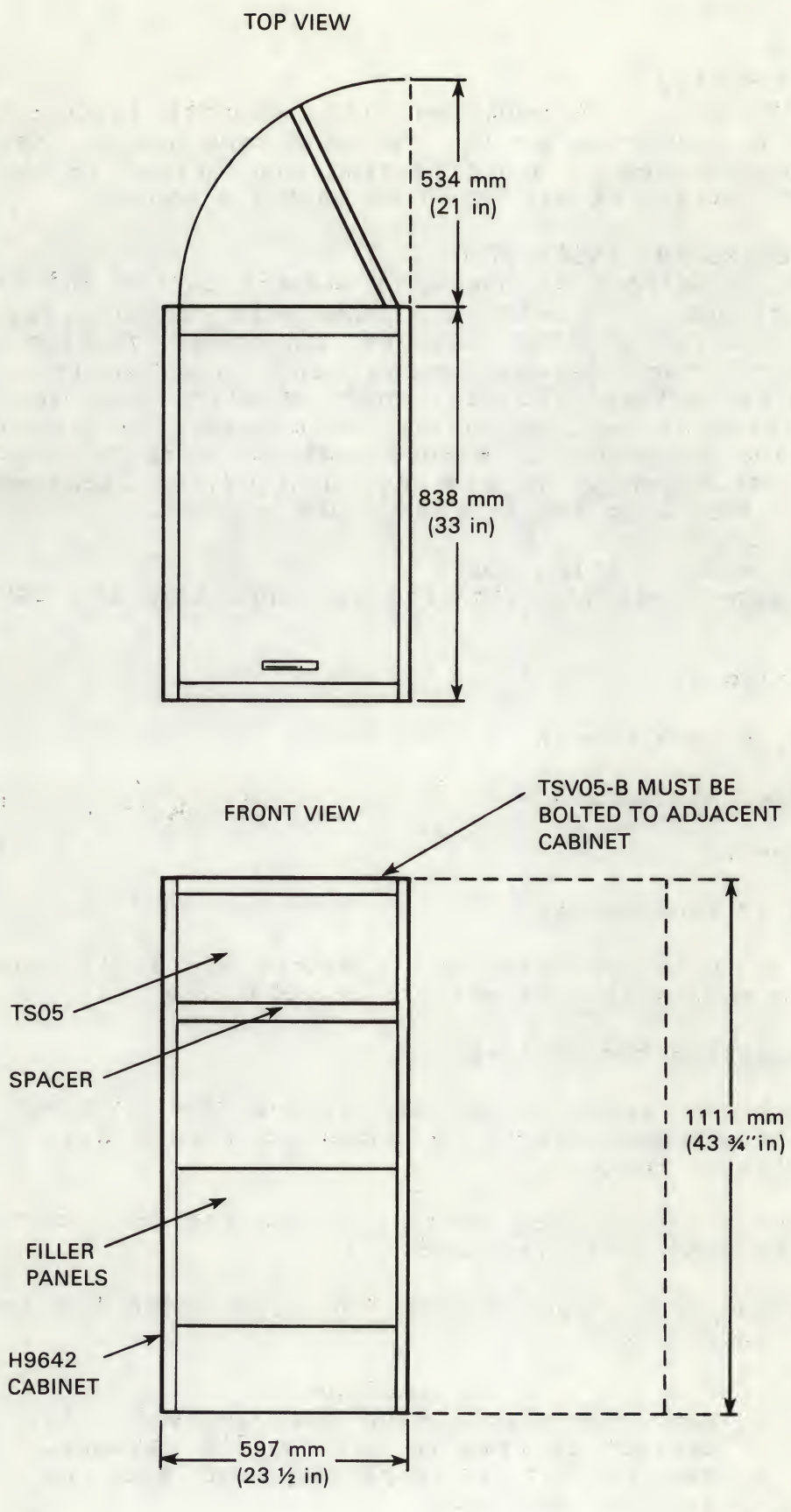


Figure 2-1 Cabinet Access Requirements

2.1.4 Air Purity

The tape transport is equipped with internal filters to prevent dust from accumulating on the tape and tape heads. Nevertheless, it is good practice to avoid placing the cabinet in the path of a dust-laden current of air (such as beside a door).

2.2 UNPACKING AND INSPECTION

The TSVØ5 is shipped as one skid-mounted carton and one or more smaller cartons. The carton on the skid contains the TSØ5 tape transport cabinet. The smaller carton(s) contain the M7196 controller, the documentation and accessories, and two individually packaged cables. These smaller items may be shipped in one carton or two, depending on shipping requirements. Check the shipping documents to ensure that the correct model has been shipped. If anything is missing, damaged, or incorrect, contact the dealer from whom the equipment was ordered.

2.2.1 Tools and Working Space

The following tools are required for unpacking the TSVØ5 subsystem:

1. Scissors
2. 9/16 inch wrench
3. 3/4 inch wrench
4. Hammer
5. 5/32 inch hex key

Also, an area of approximately 3 meters (1Ø feet) square is required for moving the cabinet off the shipping skid.

2.2.2 Unpacking the Cabinet

1. Cut the nylon straps and remove the cardboard pieces of the cabinet carton as shown in Figure 2-2. Remove the plastic bag.
2. Using a 9/16 inch wrench, remove the four bolts that hold the cabinet to the skid.
3. Slide the wooden blocks out from under the cabinet (see Figure 2-3).

CAUTION

Once the blocks have been removed, the cabinet is free to roll on its casters. The cabinet is top-heavy and must be handled with care.

The blocks may require a few taps with a hammer to move them out from under the cabinet. It may be helpful to tilt the cabinet slightly while removing the blocks.

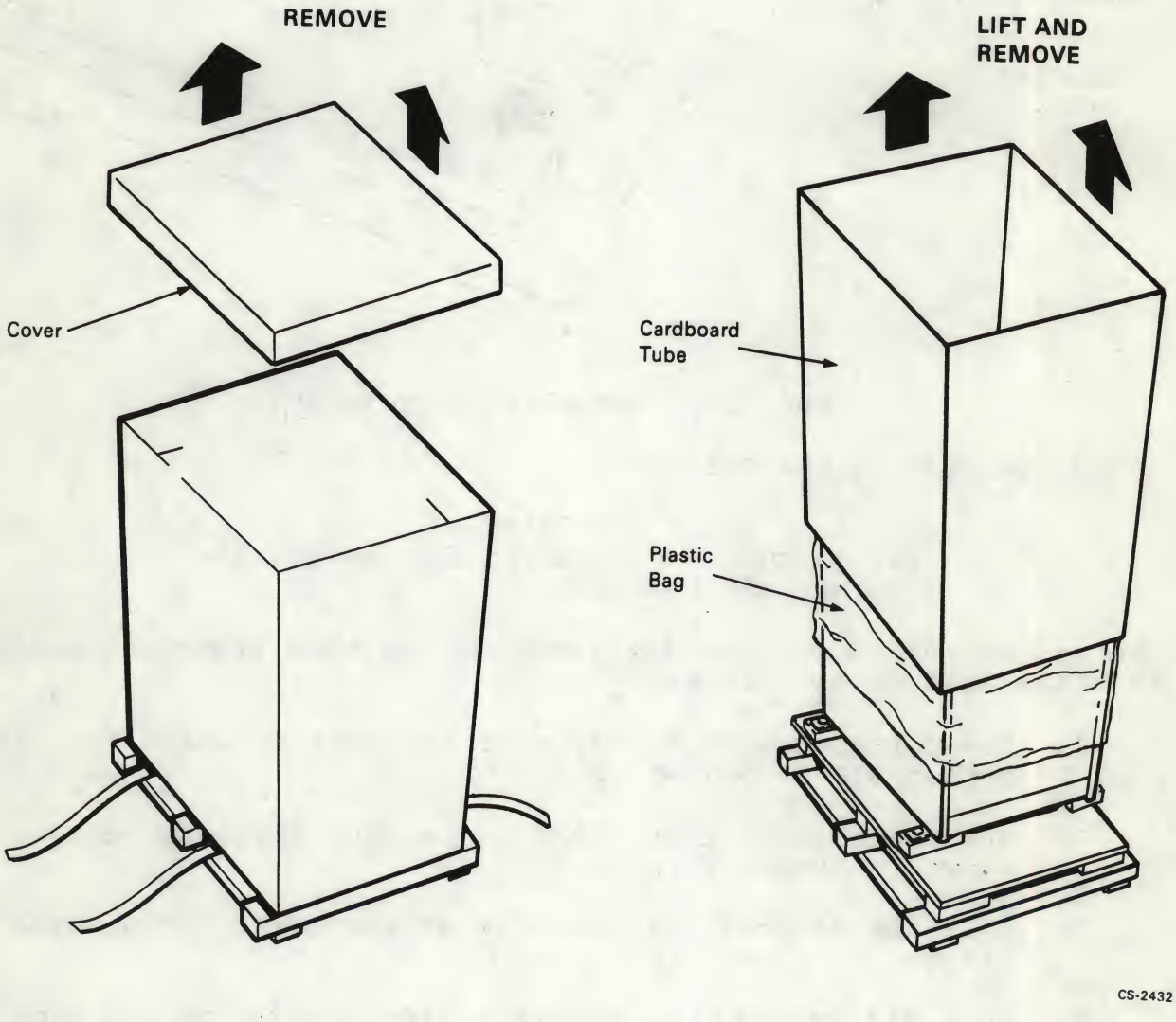


Figure 2-2 Cabinet Carton Removal

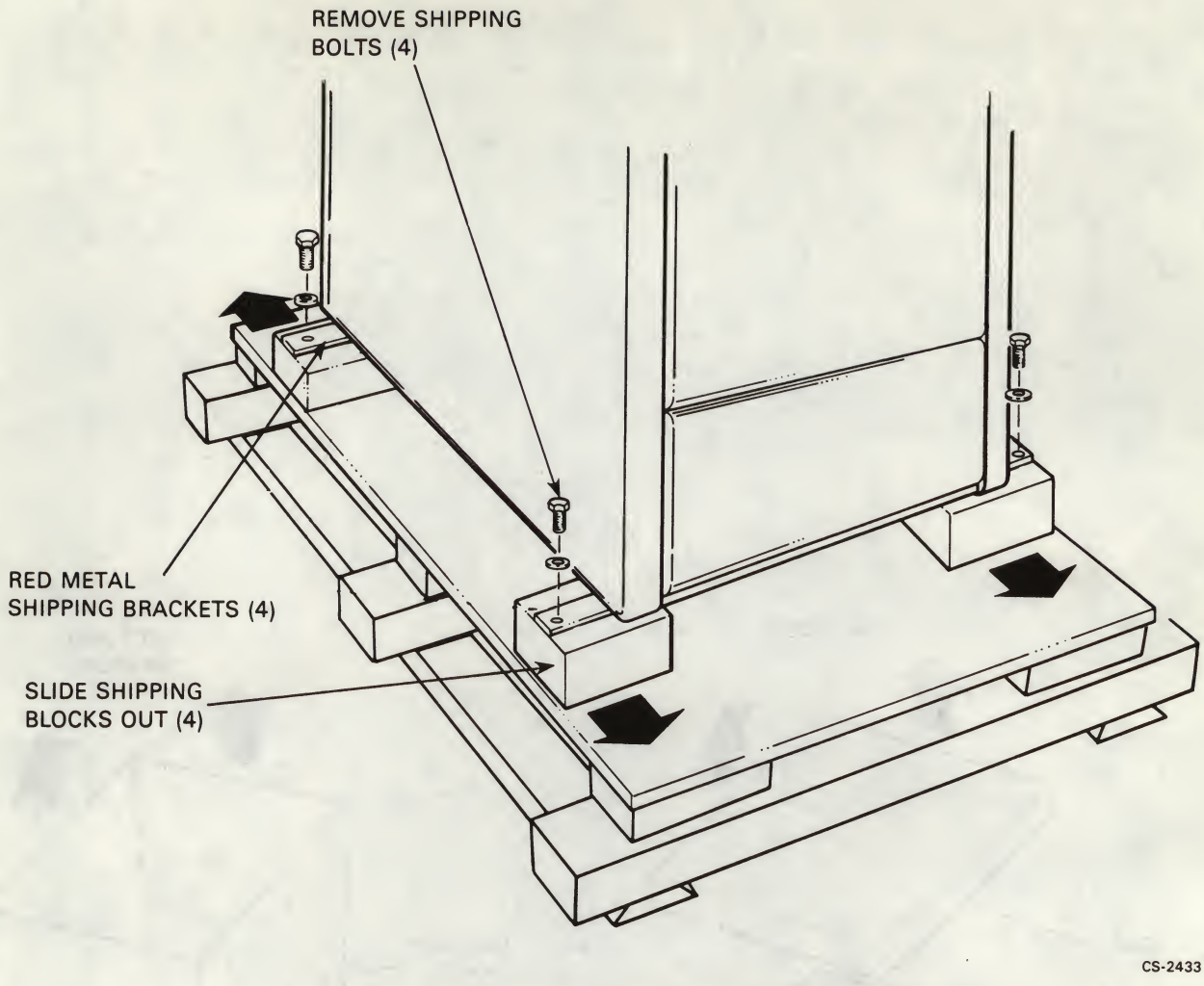


Figure 2-3 Removing Shipping Bolts

2.2.3 Deskidding the Cabinet

WARNING
Two people are required for moving the cabinet off the skid.

The recommended procedure for removing the tape transport cabinet from the skid is as follows:

1. One person stands in front of the cabinet while the other person stands behind it.

2. Grasp the cabinet by right top and by the left center, as shown in Figure 2-4.

3. Roll the cabinet off the side of the skid, taking care to prevent it from toppling over.

4. When the casters on the left side of the cabinet are on the floor, push the skid out from under the right side of the cabinet. Take care to prevent the cabinet from hitting the floor hard or toppling.

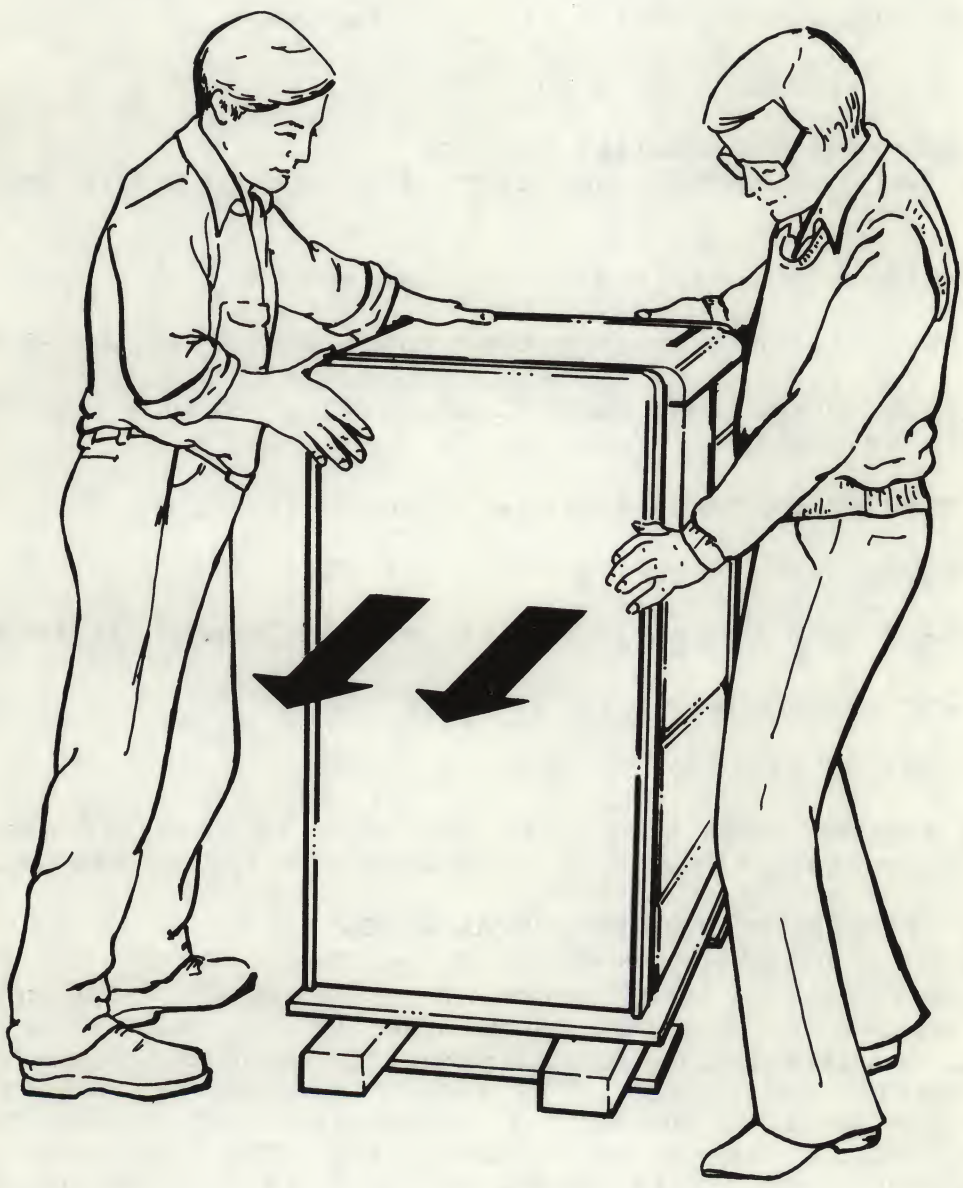


Figure 2-4 Deskidding the Cabinet

5. With the cabinet standing on the floor, use a 3/4 inch wrench to remove the red metal shipping brackets from the bottom. After they are loosened, the brackets slide outward.

6. Open the rear door using a 5/32 inch hex key (see Figure 2-6) and verify that the envelope taped to the bottom of the cabinet contains:

   a. 7008288-8F remote cable

   b. H9544-HB leveler feet and hardware

   c. 7422224/7422225 intercabinet hardware

2.2.4 Unpacking the Smaller Cartons

Open the smaller cartons and check that they contain the following:

1. M7196 bus interface/controller module

2. Two interconnection cables (part number 7016855-08)

3. TSV05 Tape Transport Installation Manual (EK-TSV05-IN) (this manual)

4. TSV05 Tape Transport User's Guide (EK-TSV05-UG)

5. TSV05 Pocket Service Guide (EK-TSV05-PS)

6. 26.7 centimeter (10.5 inch) magtape number 30-18709-08

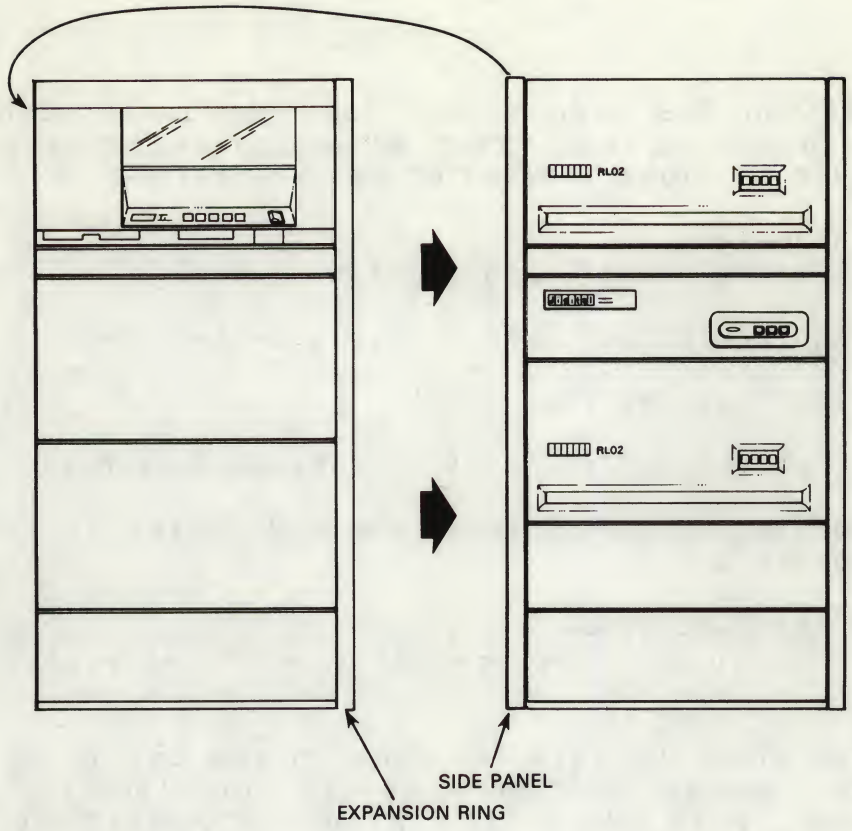
7. Tape cleaning kit part number TUC02

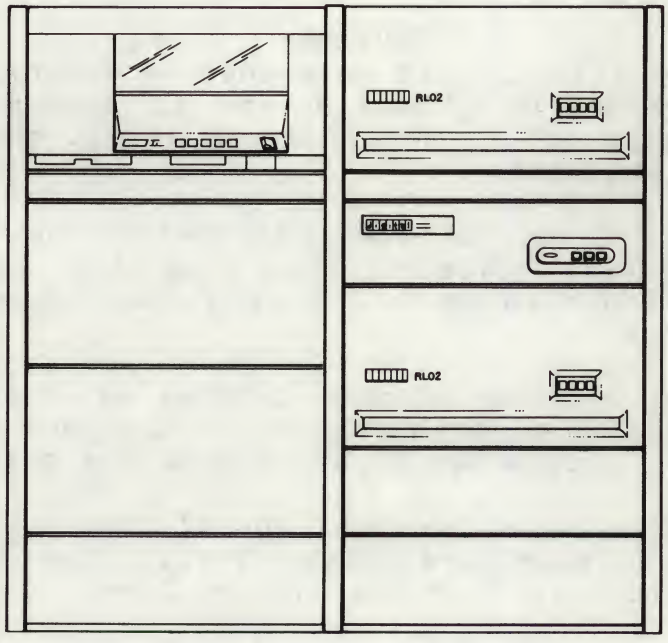
8. MP01157 field print set.

Visually inspect each item. If any item is damaged, missing, or incorrect, contact the dealer from whom the system was purchased.

2.3 TAPE TRANSPORT CABINET INSTALLATION

The TSV05 subsystem is designed to be connected to the left side of an H9642 cabinet that contains a PDP-11/23 computer. Older LSI-11 computer systems that use H9612 cabinetry require alternative installation procedures. These procedures are defined in the MP01157 print set. The tape transport cabinet is shipped with no side panels, but with an expansion ring on the right side of the cabinet. (Refer to Figure 2-5.) The left side panel of the computer cabinet is moved to the left side of the tape transport cabinet. Then the right side of the tape transport cabinet is bolted to the left side of the computer cabinet.





EXPANDED SYSTEM

CS-2436

Figure 2-5 Tape Transport Cabinet Connection

This configuration has been tested for compliance with FCC requirements. Installing the TSV05 subsystem in other configurations may result in higher levels of EMI radiation.

2.3.1 Tools Required

Cabinet installation requires the following tools:

1. 9/16 and 11/16 inch wrench (for leveling feet)
2. 5/32 inch hex key (for door)
3. 7/16 inch wrench (for bolting cabinet together)
4. Screwdriver or nut driver, as applicable, for connecting ground cable.

2.3.2 Moving the Side Panel

Install the TS05 cabinet levelers and move the side panel as follows:

1. Install the four leveling feet on the bottom of the TS05 cabinet (Refer to Figure 2-6.) The leveling feet are screwed into the holes previously used by the red shipping brackets. The cabinet must be tilted to the left to provide clearance for installing the feet on the right side, and tilted to the right while installing the feet on the left side.

   CAUTION

   Do not tilt cabinet more than necessary. Approximately 5 centimeters (2 inches) of clearance is necessary to insert the leveling feet.

2. Open the rear door of the TS05 cabinet and the CPU cabinet. Typically, this requires inserting the hex key into the latch and turning it 1/4 turn counterclockwise. (See Figure 2-7.)
3. Remove the locking bracket located at the rear bottom, right-hand side of both cabinets. Each bracket is held by two bolts. Loosen but DO NOT remove the bolts.
4. Lift the side panel straight up and remove it from the CPU cabinet left side (see Figure 2-8). Disconnect the side panel ground wire from the cabinet frame.
5. Place the side panel removed in step 4 next to the TS05 cabinet left side. Connect the side panel ground strap to the TS05 cabinet using the hardware supplied on the left rear cabinet rail.

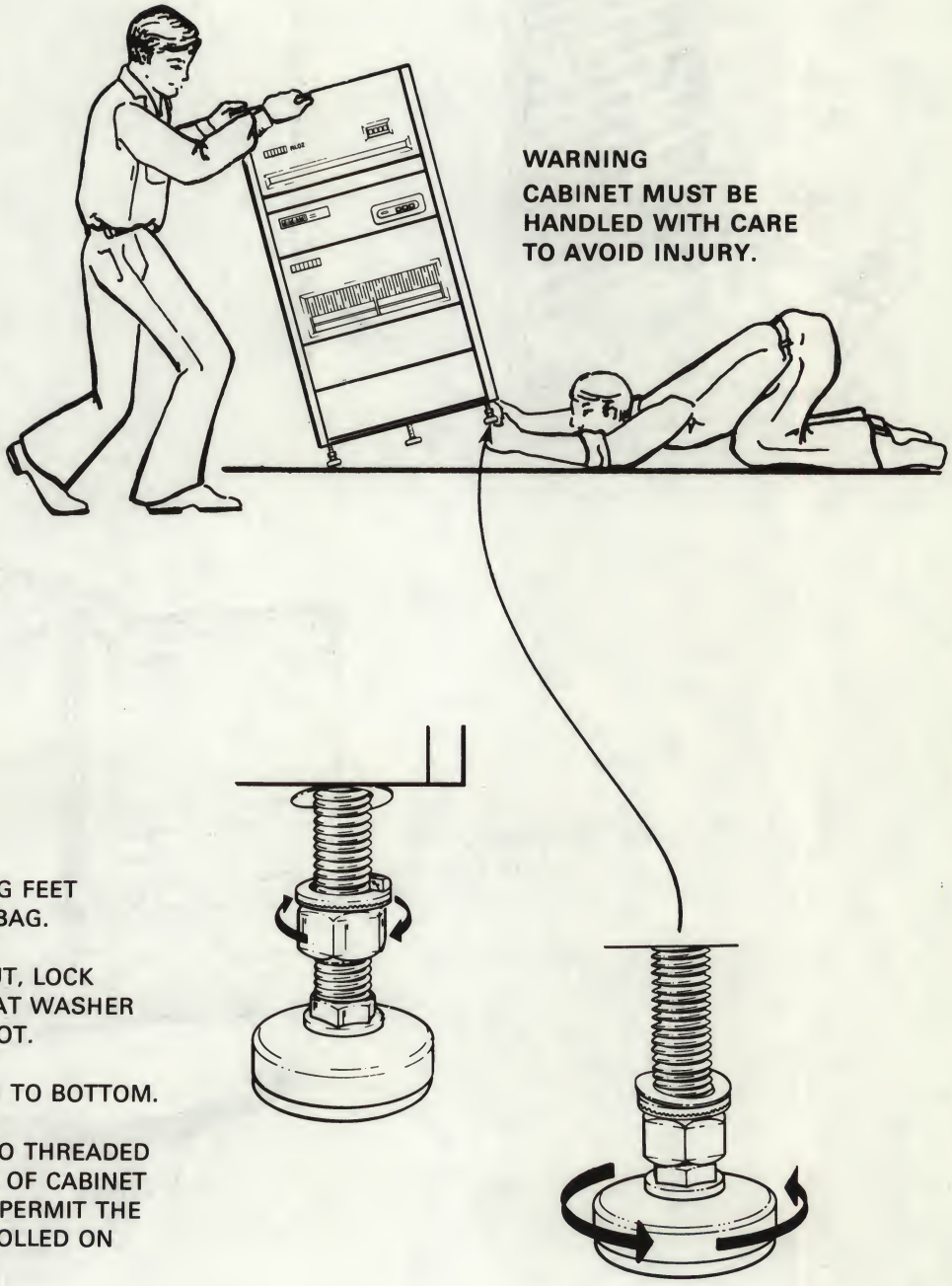


Figure 2-6 Installing Leveling Feet

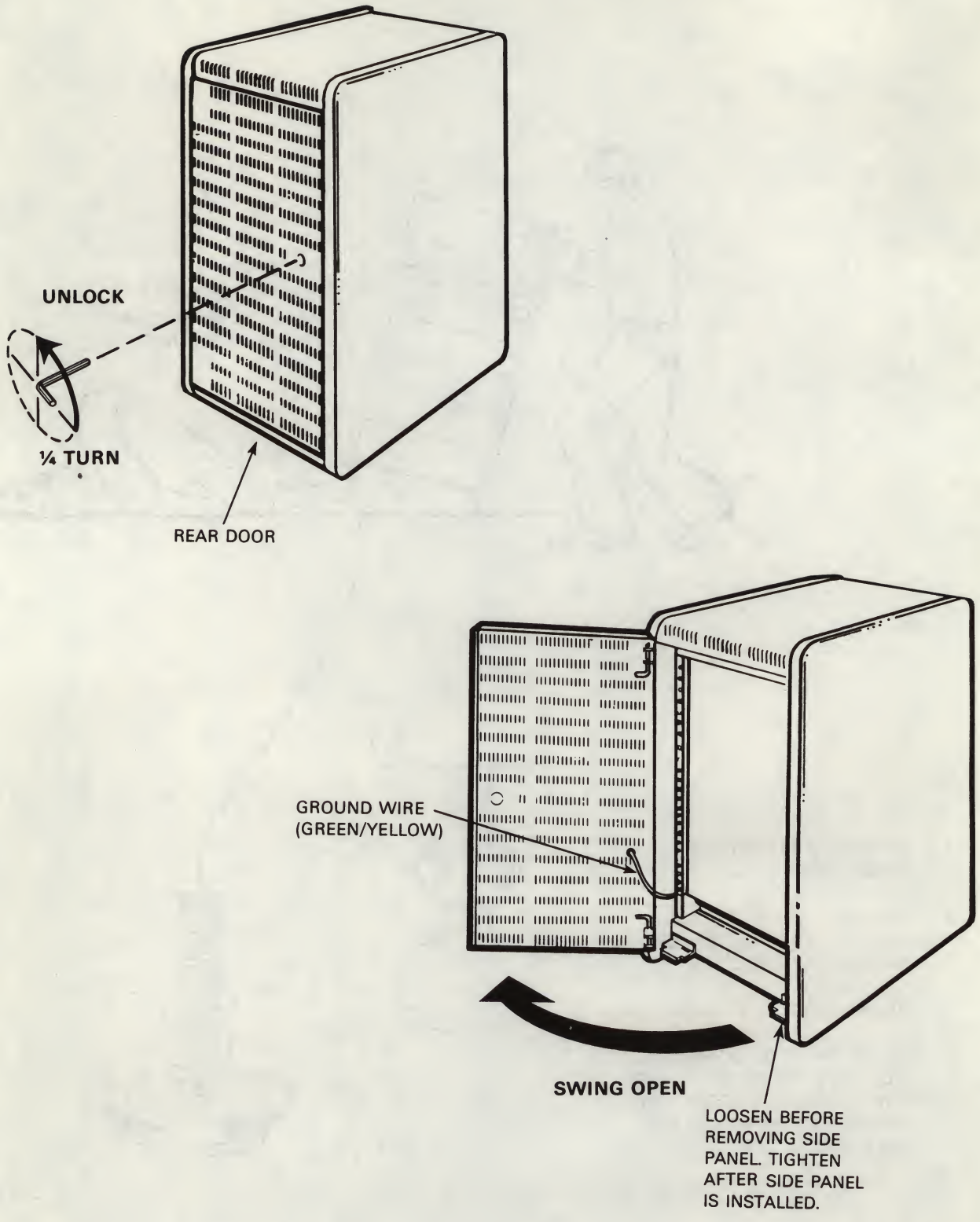


Figure 2-7 Computer Cabinet Ground Connection

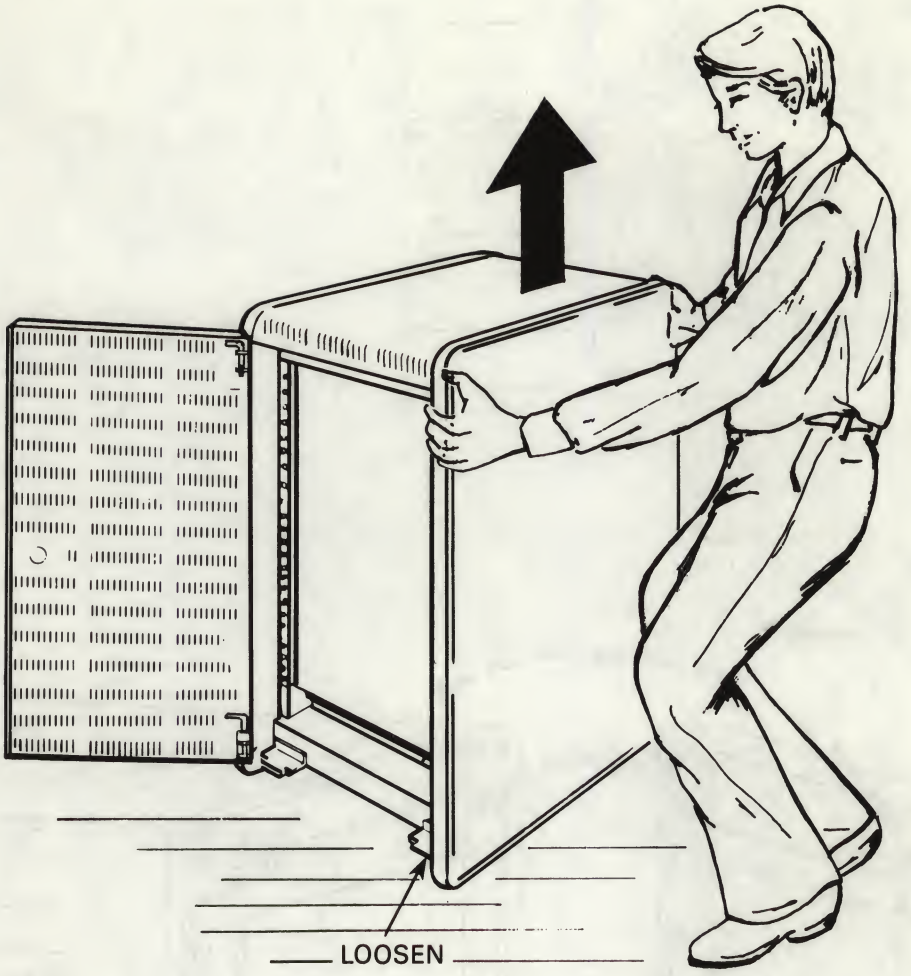
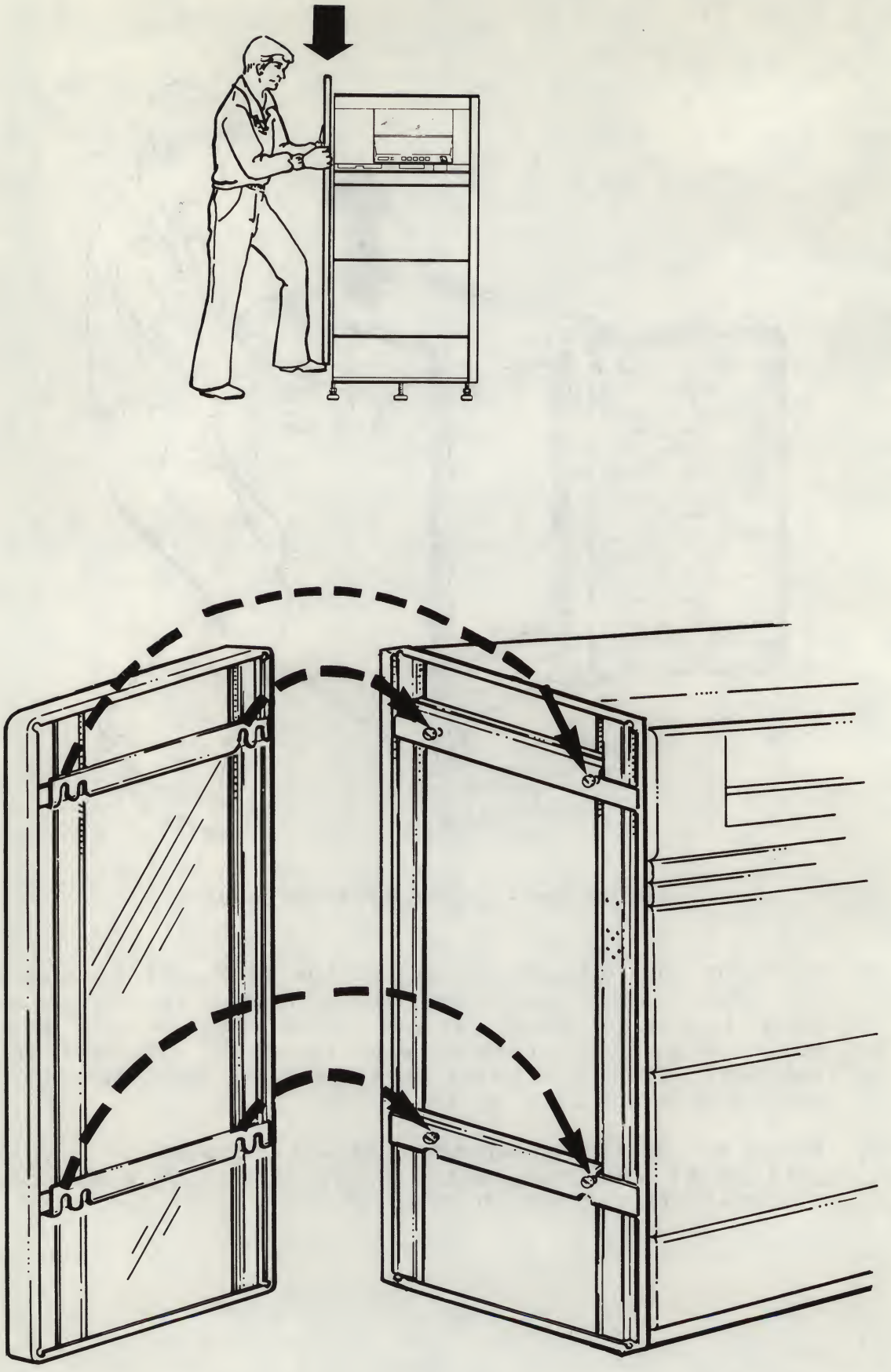


Figure 2-8 Removing Side Panel

6. Position the side panel against the TSØ5 cabinet such that the slots align with the pins. (Refer to Figure 2-9.) Hold the side panel a few inches above its mounted position until it is even with the front and rear of the cabinet. Slide the panel straight down such that the four pins engage the four slots.

7. Reinstall and tighten the bracket located on the TSØ5 cabinet at the rear bottom right side. This was one of the brackets removed in step 3.



CS-2442

Figure 2-9 Mounting the Side Panel

2.3.3 Connecting the Cabinets

The two cabinets must be connected together both mechanically and electrically. The mechanical connection is made as follows:

1. Roll the TSØ5 cabinet, with side panel attached, next to the CPU cabinet left side. Place the TSØ5 cabinet 1 inch forward of the CPU cabinet such that the pins in the CPU cabinet align with the cutouts in the trim panel. To obtain this alignment, adjust the TSØ5 leveling feet until the top of the TSØ5 cabinet is level with the top of the CPU cabinet.

2. Push the TSØ5 cabinet sideways so that it is against the computer cabinet. Push the TSØ5 cabinet backwards until it is even with the CPU cabinet. Check that all the pins are engaged properly into the trim panel. (Refer to Figure 2-1Ø.)

3. Reinstall the second locking bracket that was removed in Section 2.3.2, step 3. Do not tighten it. This bracket is located on the CPU cabinet bottom rear, right-hand side. (Refer to Figure 2-11.)

4. Loosen, but DO NOT REMOVE, the TSØ5 locking bracket that holds the rear door bottom pivot pin. This is easier if you partially remove the TSØ5 rear door by pushing down on the top pivot pin and raising the rear door out of the bottom pivot hole.

5. Install the rear intercab bracket as shown in Figure 2-11. Tighten the four screws, ensuring all brackets are fully down. Reinstall the TSØ5 rear door if it was removed in step 4.

6. Remove the bottom trim panels located on the CPU and TSØ5 cabinets. Typically, this panel is held in place by two phillips head screws.

7. Remove the four center-most bolts and two center-most trim panel brackets from the cabinetry.

8. Refer to Figure 2-11 and install the front intercab bracket. Reinstall the two trim panel brackets and tighten the four bolts, and then reinstall both bottom trim panels.

9. Recheck the cabinetry leveling. Adjust the leveling feet of both cabinets, if necessary, to ensure that the system is properly leveled and all leveling feet are properly supporting the system.

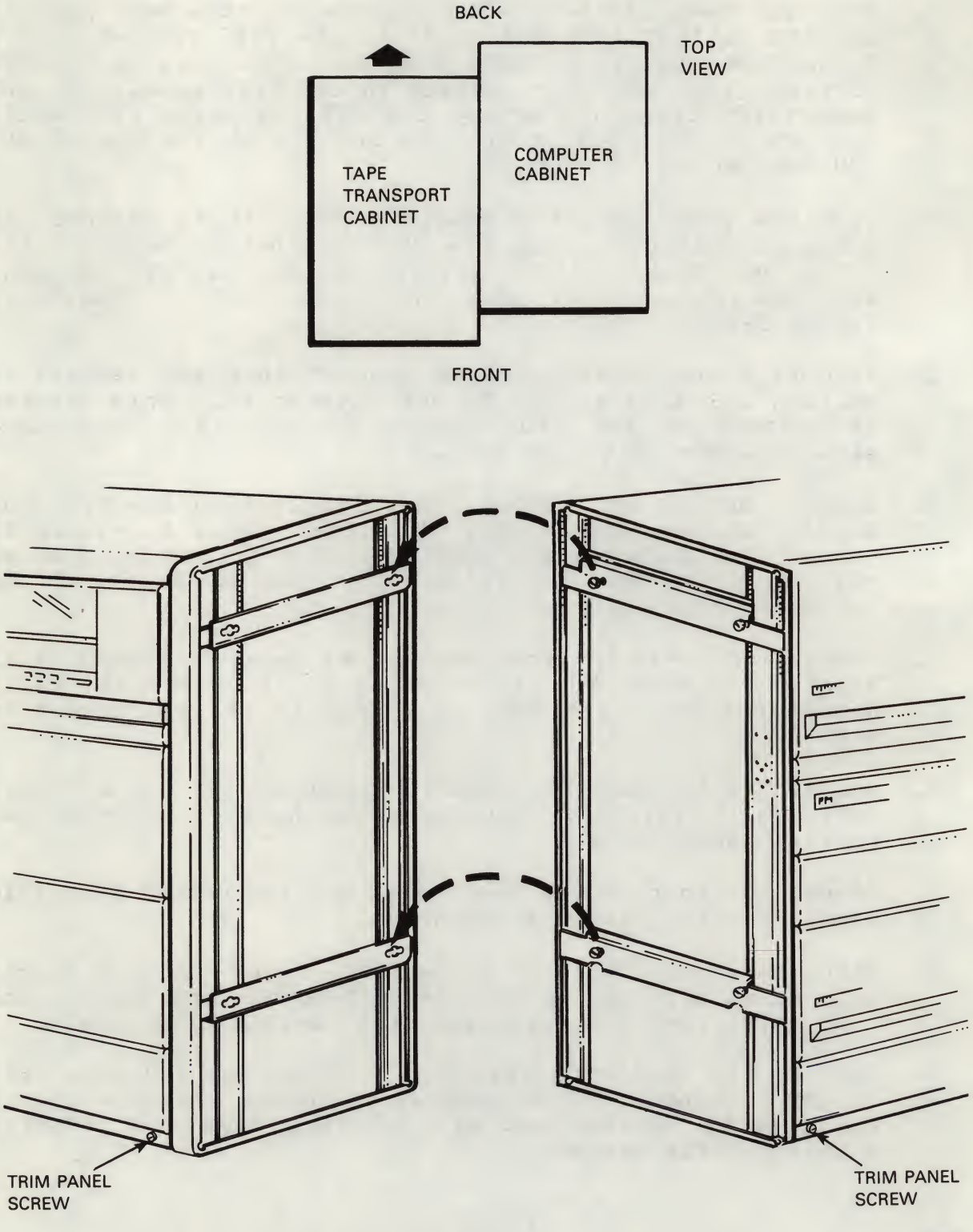


Figure 2-10 Cabinet Alignment

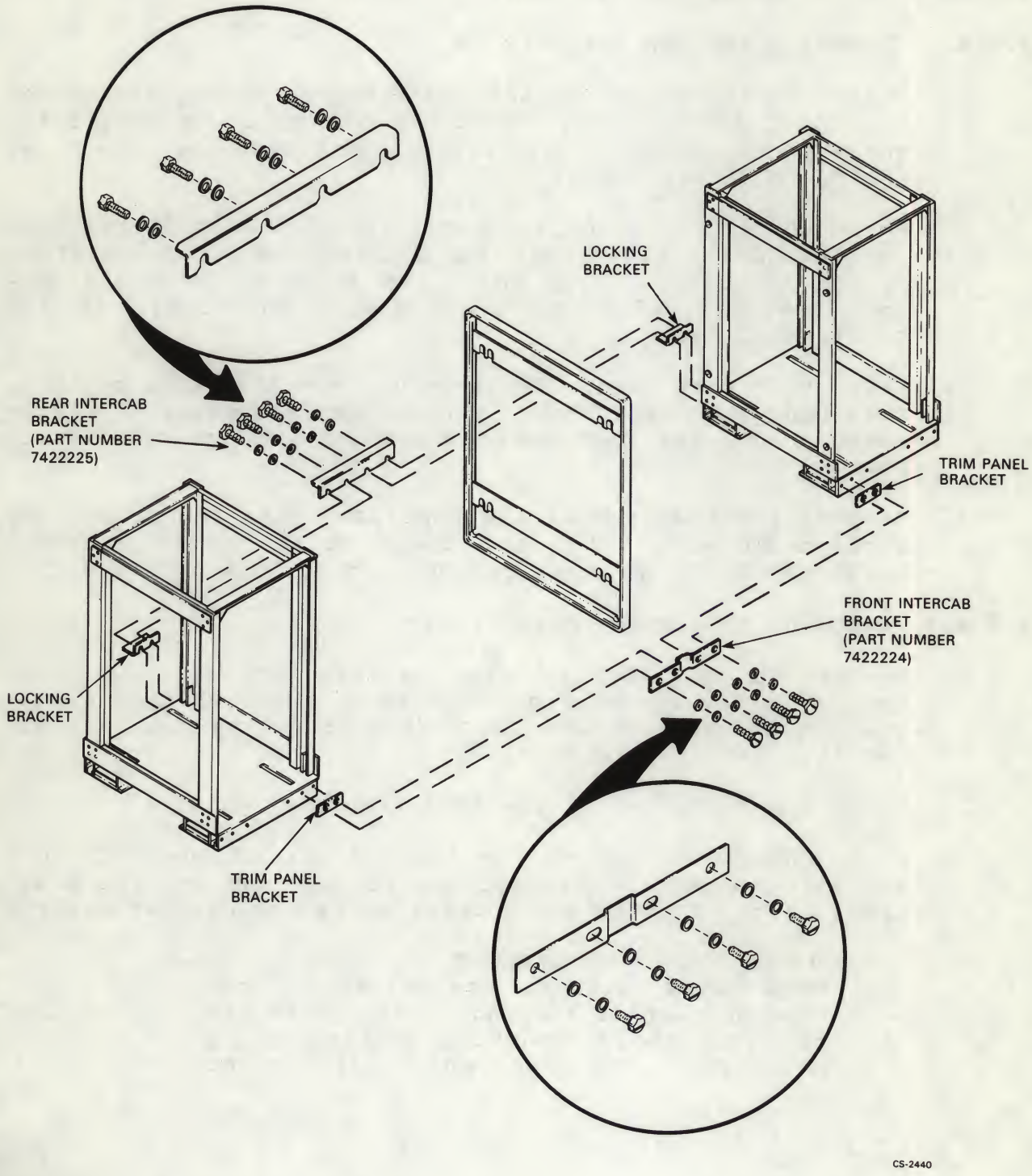


Figure 2-11 Cabinet Interconnection Hardware

2.3.4 Removing Shipping Foam

The tape transport is shipped with foam cushions protecting the takeup hub and blower motor. These cushions must be removed before the unit is powered up. This requires opening the tape transport to the operator maintenance access position to remove the foam from around the takeup hub, and opening it to the service access position to remove two other pieces of foam.

2.3.4.1 Removing the Top Foam Pieces

1. Raise the top of the cabinet by grasping the handle on the top cover and lifting. When the top cover is raised far enough, the support arm latches to keep the cover up. (Refer to Figure 2-12.)

2. Raise the top cover of the tape transport unit by reaching in through the front door and pushing upward on the front of the top cover. Prop the cover up using the nylon support that hangs from the left side of the cover. (Refer to Figure 2-13.)

3. Refer to Figure 2-14. Gently move the tachometer assembly away from the takeup hub. Remove the foam cushion. Carefully place the tachometer assembly back on the takeup hub.

4. Inspect and ensure that the tape path area is free of any foreign matter. With the cover still in the operator maintenance access position, proceed to Section 2.3.4.2.

2.3.4.2 Removing the Bottom Foam Pieces

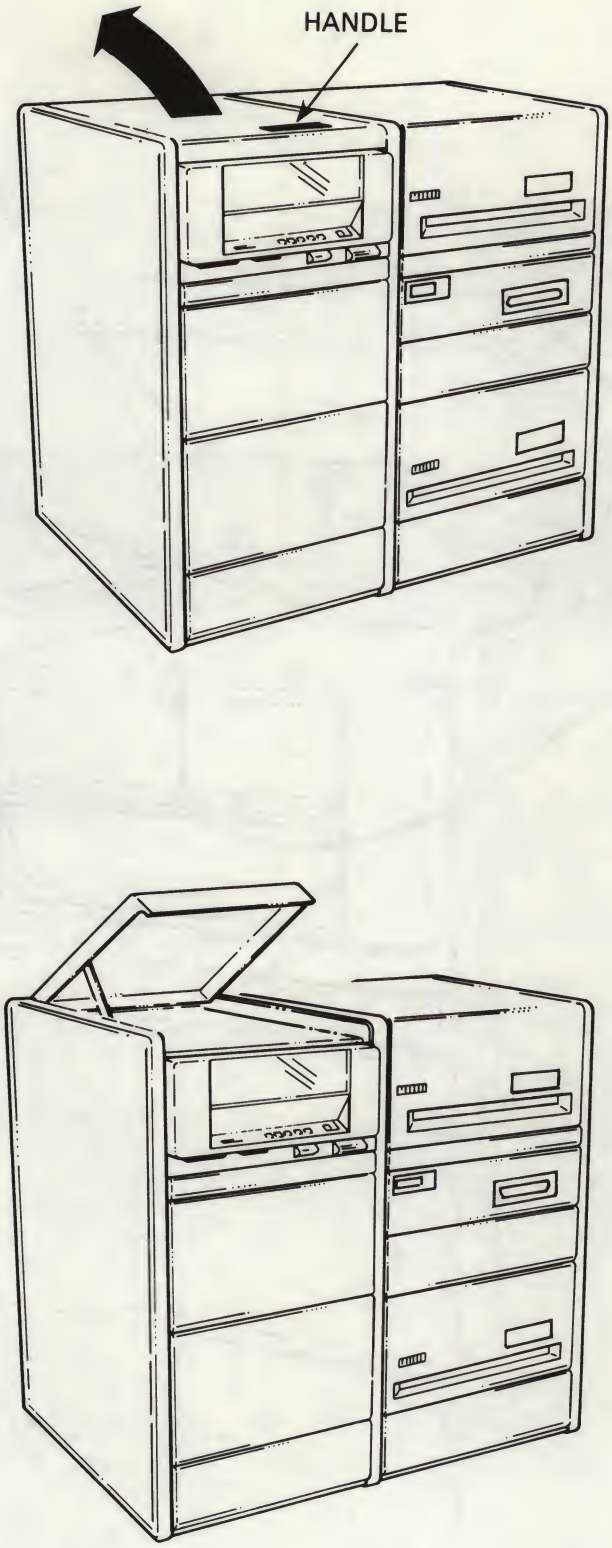
1. Loosen the two spring-loaded captive screws, located on each side (as viewed from the top of the TSØ5 tape transport unit), that secure the TSØ5 unit to the top rail assembly. (See Figure 2-15.)

2. Lower the top cover of the tape transport unit.

3. With both hands, grasp the lower front of the TSØ5 unit and lift the entire assembly to its maximum upright position. (This engages the locking mechanism automatically.)

WARNING

Keep hands clear of the corners of the tape unit while lifting. This is important to avoid brushing the mounting rails with your hands while lifting the unit.



CS-2438

Figure 2-12 Cabinet Top Cover

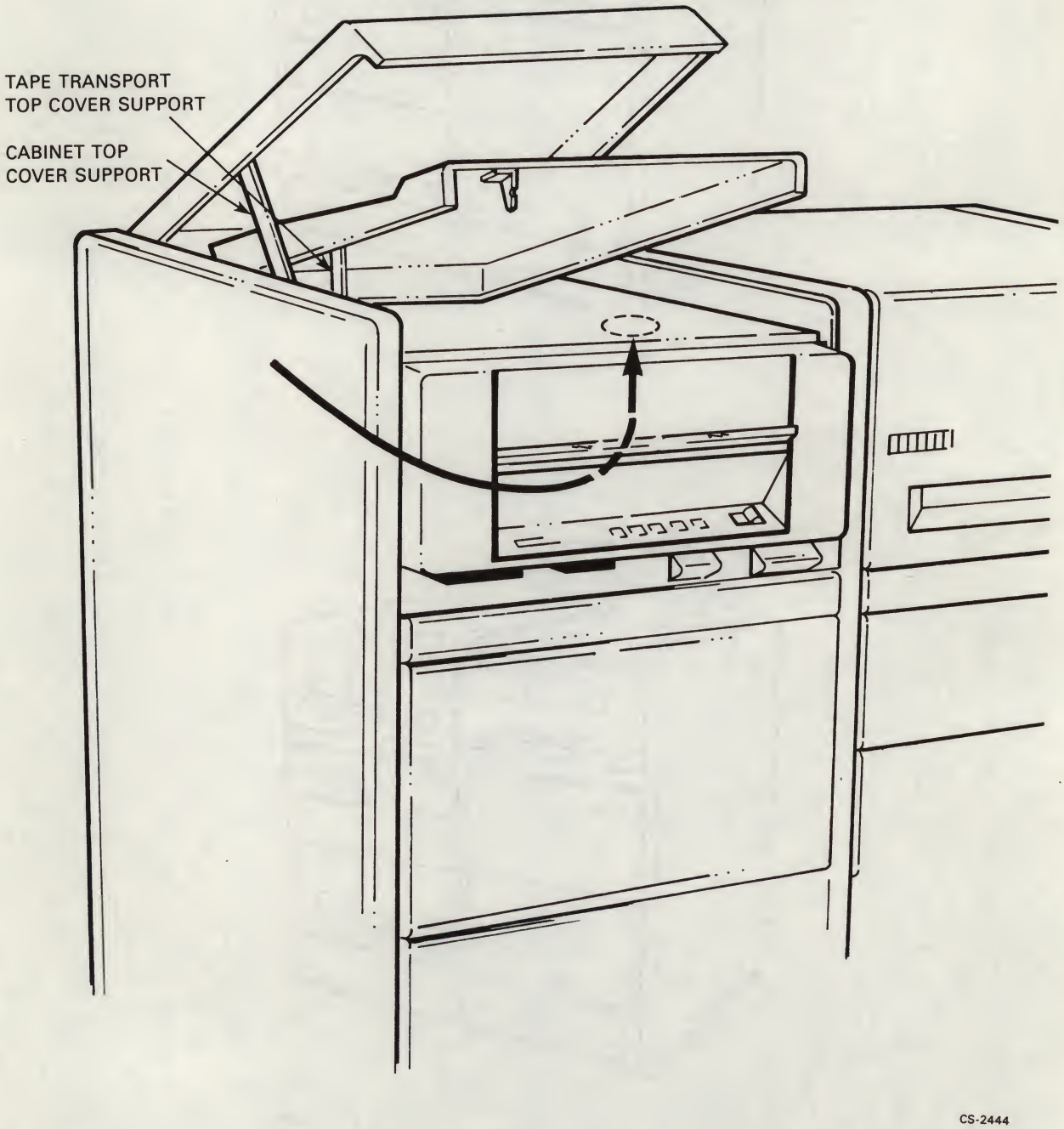


Figure 2-13 Tape Transport Top Cover

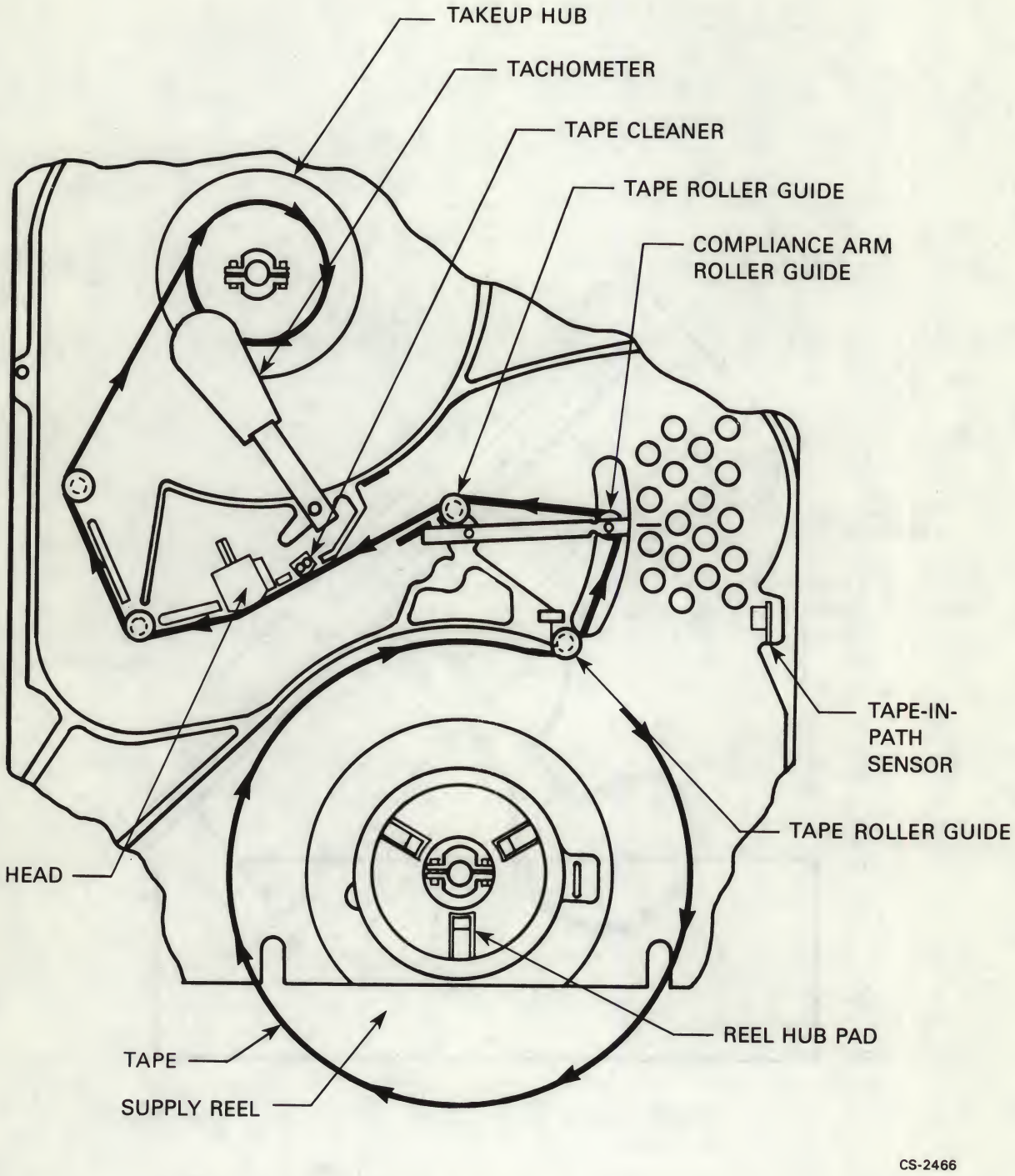


Figure 2-14 Tachometer and Takeup Hub

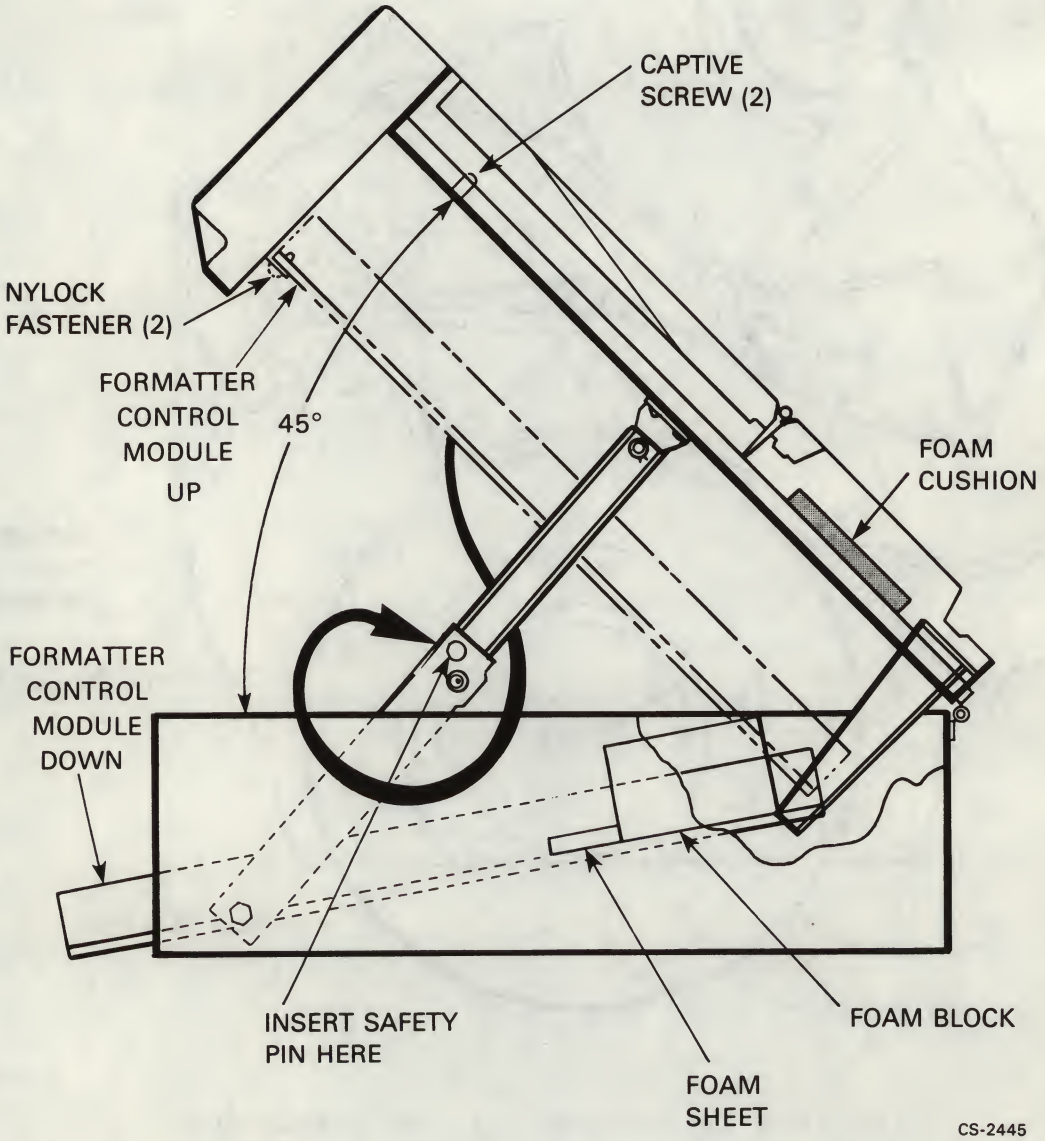


Figure 2-15 Service Access Position

4. Carefully lower the TSØ5 unit approximately 2.5 centimeters (1.Ø inch). (This will activate the locking mechanism automatically.)

WARNING

To eliminate the possibility of the tape unit dropping due to a failure in the locking mechanism, insert the supplied safety pin into the hole provided [2.5 centimeters (1.Ø inch)] above the locking mechanism on the top plate supporting slide. Route the safety pin behind the supporting slide and across in front, and install it from left to right.

5. Release the drive/formatter module by pulling down on the two Ny-Lok fasteners that secure it to the bottom of the top plate assembly. When the Ny-Lok fasteners are released, carefully lower the drive/formatter module as far as it will go.

6. Remove the sheet and block of foam from the unit.

7. Place the TSØ5 unit back to the operating position by reversing steps 1 through 5.

8. Close the top cover of the tape unit and the top cover of the cabinet.

NOTE

To release the cabinet top cover support arm, it is necessary to raise the top cover slightly and move the top of the arm forward.

2.3.5 Connecting Line Power

Before connecting the line power, perform the following checks:

1. Power switch on the front panel of the tape transport is in the Ø (OFF) position.

2. Power controller voltage rating is correct for your system.

3. Power controller circuit breaker switches are in the OFF position.

4. Power controller LOCAL/REMOTE switch is in the LOCAL position.

With the switches in these positions, unwind the power cable and plug it into the receptacle.

2.4 TAPE TRANSPORT CHECKOUT

The tape transport is tested by itself before being cabled to the bus interface/controller module. This standalone testing is performed with the line power controlled locally at the cabinet power controller. After standalone operation has been verified, operation with the computer system is tested. At that point, the tape transport cabinet power is placed under the control of computer cabinet power controller by connecting the remote control cable. For the tests in this section, however, the remote control cable remains unconnected.

2.4.1 Power Up Test

1. Switch the circuit breaker switches on the cabinet power to the ON position. Observe that the power controller pilot lamp lights. Close the cabinet rear door.

2. On the tape transport front panel (Figure 2-16), press the power switch to the 1 (ON) position. Observe that all indicators light for approximately 2 seconds.

3. Observe that after 2 seconds all the indicators extinguish, and then the UNLOAD indicator lights.

If these indications have occurred, the tape transport unit has successfully completed the internal verification checks that it performs automatically at power up. If the indications were different, there is a problem. Refer to the TSV05 Pocket Service Guide or call your local Digital representative.

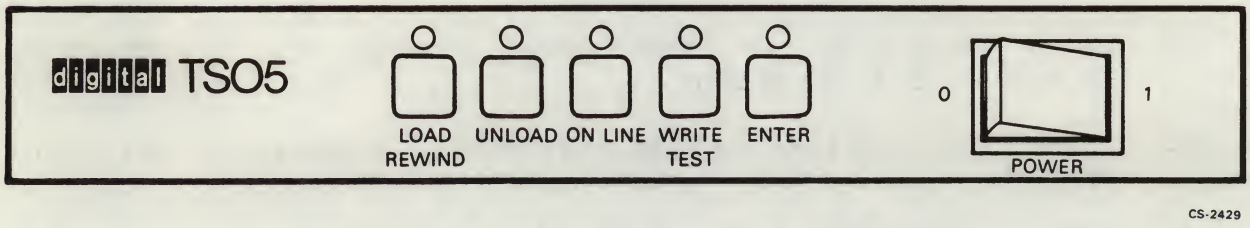


Figure 2-16 Front Panel Controls and Indicators

2.4.2 Tape Loading Test

This test verifies the ability of the TSV05 subsystem to automatically load a tape. It requires a tape that is blank except for the beginning-of-tape (BOT) and end-of-tape (EOT) markers. Refer to Figure 2-17 and proceed as follows:

1. Ensure that the tape is wound completely onto the reel and that the end has been properly crimped.

2. Open the front panel door by gently pressing down on the top center area of the door.

3. Hold the tape with the file-protect ring side down, and insert it into the transport unit, centering it on the hub.

4. Close the door.

CAUTION

Both the tape transport top cover and the front panel door are locked when a tape is loaded. Any attempt to force open either the cover or the door before the tape is unloaded will result in mechanical damage to the locking mechanism.

5. Press the LOAD switch. This locks the cover and the door and begins the loading sequence.

6. Observe the LOAD indicator. It blinks while the tape is being loaded. After a maximum of 135 seconds, it stops blinking and remains lit. This indicates that the tape loading sequence is complete.

   If the LOAD indicator does not stop blinking, or if the other indicators begin to blink, there is a problem. Unload the tape, check for a proper crimp, and retry the test. If the tape does not load, refer to the TSV05 Pocket Service Guide or to the manual loading instructions in Appendix B.

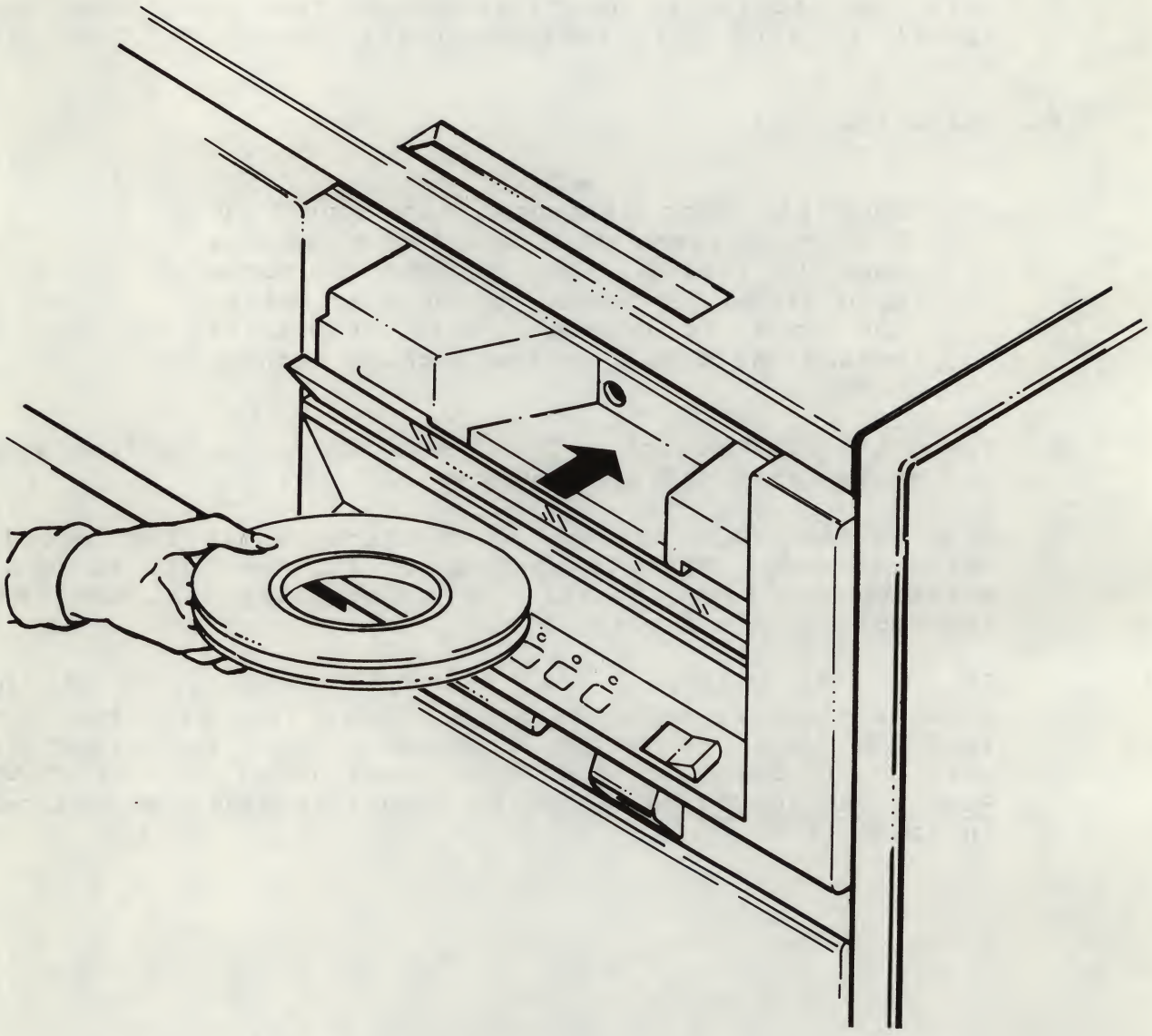


Figure 2-17 Inserting Tape

2.4.3 Tape Movement Test

This test exercises the tape drive in both forward and reverse directions and at both high and low speeds.

NOTE

If you make an error and enter an illegal test sequence, or if you stop during the sequence and permit more than 2 seconds to pass before pressing the next switch in the sequence, the system aborts the test instruction and you must start the sequence from the beginning. An erroneous or aborted test instruction results in an expanding pattern of blinking.

1. Start the test by pressing the front panel control switches in the following sequence:

   a. TEST

   b. ENTER

   c. UNLOAD

   d. UNLOAD

   e. ENTER

2. The tape should begin to move after step e.

3. Observe the indicators. If, over a period of 2 minutes, they change their blinking value substantially, there is a problem. If the blinking remains about the same, the test is progressing successfully.

4. After 2 minutes, terminate the test by pressing the TEST key. This causes the tape to rewind (which may take several minutes) and the LOAD indicator to light.

If problems are encountered, refer to the TSV05 Pocket Service Guide.

2.4.4 Tape Unloading Test

This test verifies the ability of the tape unit to unload the tape automatically.

1. Press the UNLOAD switch.

2. Observe the UNLOAD indicator. It blinks to indicate that the tape is being unloaded. When the unloading process is complete, the UNLOAD indicator lights continuously, and the front panel door and top cover are unlocked. This should take a maximum of 15 seconds.

3. Open the front panel door and lift the tape reel out of the tape transport.

4. Close the door.

5. Press the tape transport power switch to the Ø (OFF) position.

6. Switch the circuit breaker switches on the cabinet power controller to the OFF position.

2.5 BUS INTERFACE/CONTROLLER MODULE INSTALLATION

The M7196 bus interface/controller module plugs into a quad slot in the LSI-11 backplane. It connects to the LSI-11 bus on the A and B sets of edge connectors (module fingers). It is shipped with the DIP switches set for an interrupt vector of 224 and for addresses of 772520 and 772522. If your system already uses any of these addresses, the M7196 module must be switched to other addresses. Refer to Appendix A for information on switching the DIP switchpacks on the M7196 module. Refer to the Microcomputers and Memories Handbook or your system configurator for guidance in selecting new addresses.

For guidance in choosing the best backplane slot in which to install the M7196 module, refer to your system documentation or to the Microcomputers and Memories Handbook.

Install the M7196 module as follows:

1. Test the computer system to verify that it is functioning properly.

2. Power down the computer system.

3. Remove the cover to gain access to the backplane. (Which panel must be removed depends on which system you have. Earlier systems accept modules in the front, while in more recent models the modules are inserted in the back. Refer to your system documentation.)

4. Insert the module into the LSI-11 backplane. Do not fully seat the module until the cables have been installed.

2.6 CABLE INSTALLATION

Cable installation involves connecting the M7196 module to the tape transport unit and connecting the tape transport cabinet power controller to the computer cabinet power controller.

2.6.1 M7196 Module and Tape Transport Interconnection

Each of the two flat interconnection cables has a large connector on one end and a small connector on the other end. The large connectors go to the tape transport unit and the small connectors to the M7196 module. Refer to Figure 2-18 and proceed as follows:

1. Take a cable and position it so that pin 1 of the smaller, "low profile" connector lines up with pin 1 of connector J1 on the M7196 module. Pin 1 on the cable connector is indicated by a red stripe on the cable.

2. Gently push the cable connector into the J1 module connector until it is seated.

3. Route the cable to the rear of the cabinet. Cable routing depends on the model and configuration of the computer system, however, try to avoid blocking ventilation or running the cable where it may get caught on other equipment when a chassis is pulled out. Refer to drawing UA-TSVØ5-B for typical cable routing.

4. Pass the cable through the open side of the computer cabinet and into the tape transport cabinet. Do not route the cables outside the cabinetry.

5. Refer to Figure 2-19. Line up pin 1 of the cable connector with pin 1 of connector P1 on the tape transport unit. There are two sets of connectors on the back of the tape transport unit. The TSVØ5 subsystem uses the left-hand set of connectors.

6. Gently press the cable connector onto the P1 edge connector in the back of the tape transport cabinet.

7. Repeat this procedure to cable J2 of the M7196 module to P2 of the tape transport unit. Ensure that pin 1 of J2 connects to pin 1 of P2.

8. After both interconnection cables have been installed, fully seat the module.

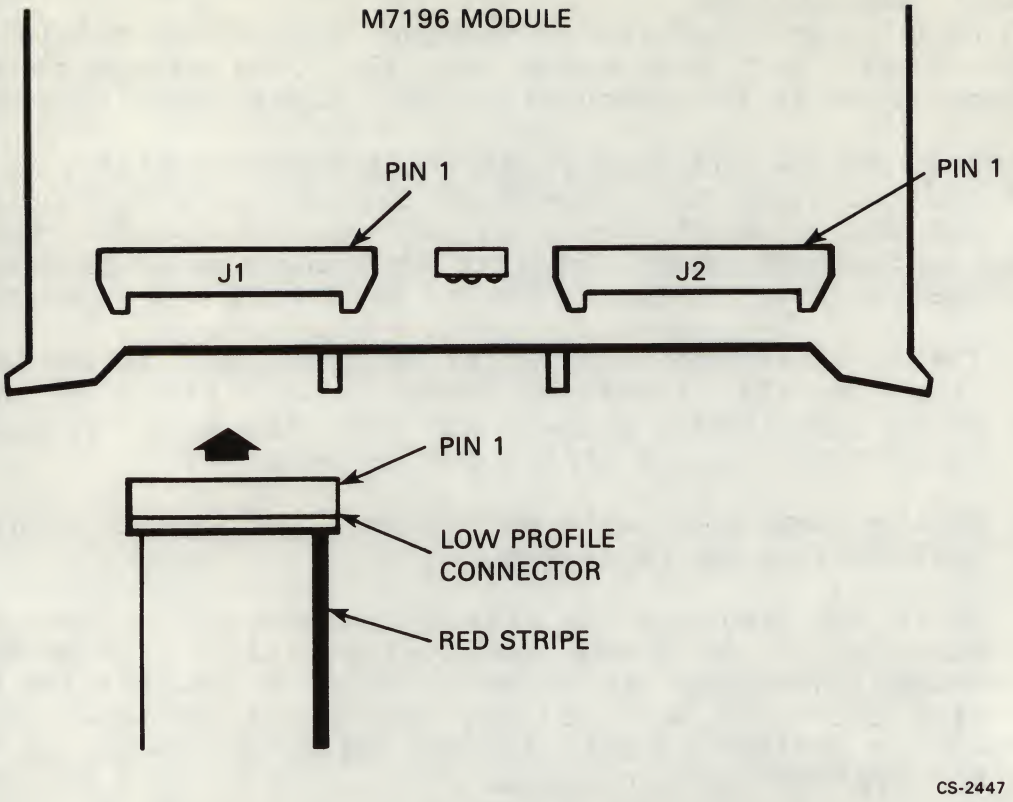


Figure 2-18 Cabling the M7196 Module

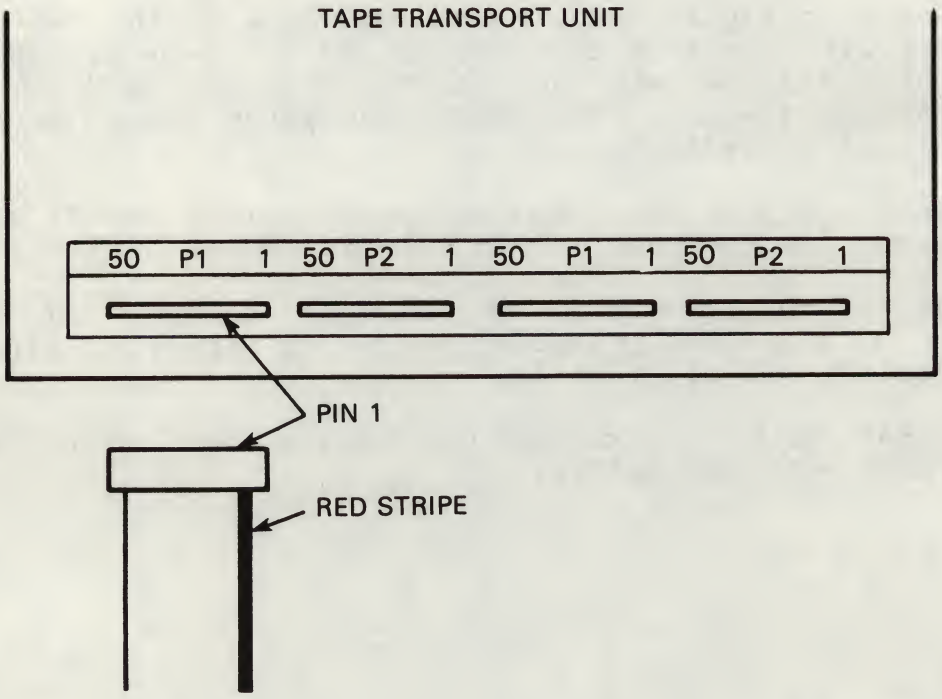


Figure 2-19 Cabling the Tape Transport

2.6.2 Power Controller Interconnection

The power controllers in the two cabinets are to be interconnected by a remote control cable. This enables the computer cabinet power to switch on the tape transport cabinet power automatically whenever the computer is powered up.

The remote control cable, part number 7008288-8F, has a three-pin connector on each end. The cable connectors are the same, and they are keyed to plug in only one way. Refer to Figure 2-20 and install the remote control cable as follows:

1. In the computer cabinet, plug one end of the cable into the power controller connector labeled DEC POWER CONTROL BUS.

2. Route the remote control cable through the open side of the computer cabinet and into the tape transport cabinet. Do not route the cable outside the cabinetry.

3. In the tape transport cabinet, plug the cable into the power controller connector labeled DEC POWER CONTROL BUS.

4. Place the LOCAL/REMOTE switch in the REMOTE position.

5. Switch the circuit breaker switches to the ON position.

The tape transport cabinet power is now fully interconnected with the computer cabinet.

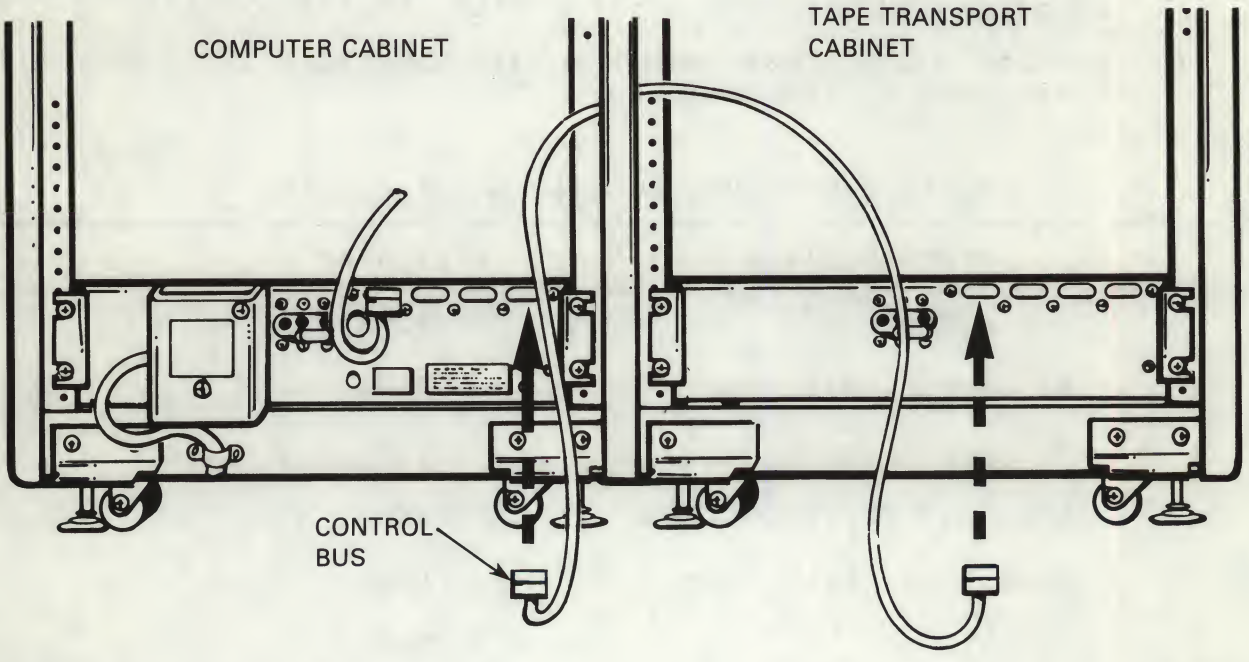


Figure 2-20 Remote Power Control Connections

2.7 TSVØ5 SUBSYSTEM CHECKOUT

The TSV05 subsystem is tested by checking the M7196 LED indicators and voltage supply, and by running the diagnostic programs listed in Table 2-2. These programs are available on the XXDP+ diagnostic software package that is shipped with the computer system. If your system is an earlier model and has the XXDP package instead of the XXDP+, contact your local Digital representative for ordering information.

2.7.1 Power Up Checks

1. Set the power switch on the tape transport unit to the ON position.

2. Switch on the computer system power and observe that the tape unit powers up with the system.

3. After a few seconds, all the tape unit indicators should be extinguished except for the the UNLOAD indicator.

4. Verify that the +5 V power to the M7196 module is within specification. Typically, the additional load of the M7196 module lowers the power supply voltage slightly. Adjust if necessary.

5. On the M7196 module, verify that the center LED (D2) is blinking. This indicates that the M7196 module self-test diagnostics are running. If other indications occur, there is a problem. Refer to the TSV05 Pocket Service Guide or contact your local Digital representative.

6. Replace the access panel on the computer and close the rear doors of the cabinets.

Table 2-2 TSVØ5 Subsystem Diagnostics

Program Title	File Name
Logic Test	CVTSAA
Advanced Logic Test	CVTSBA
Transport Test	CVTSCA
Advanced Transport Test	CVTSDA
Data Reliability Test	CVTSEA
DEC-X11	XTSAAØ

2.7.2 System Setup

1. To prevent erroneous error indications, ensure the tape transport is clean and the blank tape is of known good quality.

2. Load the blank tape into the tape transport by:

   a. Opening the front panel access door.

   b. Inserting the tape reel, with the file-protect ring side down, and centering it on the hub.

   c. Closing the door.

   d. Pressing the LOAD switch.

   e. Waiting for the LOAD indicator to stop blinking and stay on continuously.

   f. Pressing the ON-LINE switch.

3. Load the computer system diagnostic diskpack or floppy.

4. Before running the tape subsystem diagnostics, run the system exerciser or diagnostics to verify that the computer is operating properly. For instructions on running the computer system tests, refer to the documentation for the system.

NOTE

The logic test and the advanced logic test (CVTSAA and CVTSBA) do not require a tape to be loaded in order to run. The other diagnostics, however, require the tape to be loaded and the tape subsystem to be ON-LINE.

2.7.3 TSVØ5 Logic Test

This program tests the logic on the M7196 bus interface/controller module. It checks the microprocessor, RAM, and various registers. It verifies that the computer can move data out to the module and receive status in from the module. After you have booted the XXDP+ disk (DL, DX, or DY) and answered the questions about the date, the processor, and the power line frequency, start the logic test as follows (operator responses are underlined):

.R VTSA?? <CR>

The system responds with a display similar to the following:

```
DIAG. RUN-TIME SERVICES
CVTSA-A-Ø
****TSVØ5 LOGIC DIAGNOSTIC****
UNIT IS TSVØ5
DR>
```

At this point, type in the following commands:

```
DR> START/FLAG:PNT:HOE <CR>
```

This instructs the program to start the test, display the test number as each of its 11 tests are executed, and halt it if an error is detected. The computer now asks:

```
CHANGE HW (L) ?
```

Type in a "Y" for yes:

```
CHANGE HW (L)? Y <CR>
```

The computer then asks:

```
# UNITS (D) ?
```

Type in a "1" to indicate that there is one tape unit:

```
# UNITS (D) ? 1 <CR>
```

The computer than displays the device address, the interrupt vector, and the interrupt priority. If you have left the M7196 module in the configuration in which it was shipped, respond to these queries by typing a carriage return:

```
UNIT Ø
DEVICE ADDRESS (TSBA/TSDB) (O) 172520? <CR>
INTERRUPT VECTOR (O) 224? <CR>
```

If, on the other hand, you have changed the DIP switchpack settings on the M7196 module, then you must type in the parameters you selected.

The computer then asks if you wish to change the software parameters:

```
CHANGE SW (L) ?
```

For the subsystem checkout, the answer to this question is no:

```
CHANGE SW (L) ? N <CR>
```

After you have responded to these questions, the program starts testing the subsystem. The program runs continuously, repeating itself until it detects an error or until you halt it. If the program halts because of an error, refer to the CVTSAA TSV05 MAGTAPE Diagnostic User's Document for a detailed description of the tests. For assistance, contact your local Digital Field Service office.

After the program has made one pass through all the tests, halt it by pressing CONTROL C. This passes control of the system back to the diagnostic supervisor program. Then type "EXIT" to get back to the system monitor:

```
^C
DR> EXIT <CR>
.
```

2.7.4 Advanced Logic Test

This program verifies that the M7196 module can get status and write characteristics from the computer memory, and that it can deposit message packets in the computer memory. It tests error detection circuits and verifies that the computer can ititialize and write into the controller RAM memory. It checks the internal timers, buffers, and status and control logic. Also, it verifies that the controller can move signals to and from the cables that connect it to the tape transport unit.

Load this program as follows:

```
.R VTSB?? <CR>
```

After the program title is displayed and the diagnostic supervisor returns the DR prompt, enter the command line:

```
DR> START/FLAG:PNT:HOE:UAM <CR>
```

The program responds by asking the same questions about hardware and software parameters as were asked by the logic test. Type in the same answers. After the last question is answered, the program starts running its tests (this one has 12 tests, with the last 3 not executed). It runs continuously until there is an error or until you halt it. After one pass, halt the program by typing CONTROL C, and type "EXIT" to return to the system monitor:

```
^C
DR> EXIT <CR>
```

2.7.5 Tape Transport Test

This program verifies correct tape motion command decoding. It checks the basic operation of the rewind positioning command, the write data command, and the read forward and read reverse commands. It verifies that the system can space over records forward and in reverse direction, and that it can reread records. The

ability of the subsystem to respond to error conditions is also tested. The program checks the commands for retrying to write data and tape marks. It also tests the skipping of tape marks in forward and reverse directions.

Load the program as follows:

.R VTSC?? <CR>

After the system displays the program title, enter the same command line and answers to the parameter questions as for the previous program (described in Section 2.7.4). After one successful pass of the eight tests in this program, halt the program and exit to the system monitor.

2.7.6 Advanced Tape Transport Test

This program verifies the funtioning of the No-Op, Initialize, and Erase commands. It checks that errors are indicated when no data is found on the tape and it tests the data parity checking circuitry in both the controller and the tape transport electronics. It checks for the proper handling of the EOT status and tests the record buffering functions. It also checks that records and gaps written on the tape are the correct length.

Load the program as follows:

.R VTSD?? <CR>

After the title is displayed, enter the commands:

DR> START/FLAG:PNT:HOE <CR>

The program starts and runs its nine tests. After one successful pass, halt the program and exit to the system monitor.

2.7.7 Data Reliability Test

This program exercises and verifies the correct completion of all tape transport functions. It executes read and write commands a random number of times, with records of random length and data, for the entire tape.

Load the program by typing:

.R VTSE?? <CR>

and then, after the title is displayed, enter:

DR> START/FLAG:PNT:HOE <CR>

NOTE

Magtape media typically will have several flaws per reel that will cause this diagnostic to indicate write errors or write retries due to bad tape spots. These types of errors do not indicate a problem with the subsystem.

The program then asks:

SELECT DRIVE Ø-1 (Ø)?

Answer by typing Ø and a carriage return:

. Ø<CR>

2.7.8 Additional Testing

The tests described in the preceding sections provide a high confidence level that the TSVØ5 subsystem is functioning correctly. More exhaustive checks are available by allowing the diagnostic programs to run for more than one pass. The second pass of the program is more comprehensive than the first pass. All iterations after the first pass are the same, however, they are substantially longer than the first one. Running tests that cause tape motion for extended periods will require transport cleaning to prevent erronous error reports. The logic type tape motion tests, when run continuously, can cause high tape wear to occur in the first few feet of tape. In these cases, errors due to faulty or worn tape do not indicate a failure.

Another test that may be run is the DEC/X11 runtime system exerciser. This test exercises the entire system to verify that there are no spurious interactions between various subsystems and components. There is an exerciser program module for each major system component, and these are linked together to create a system exerciser that is tailored to your system. The DEC/X11 module for the TSVØ5 subsystem is XTSAAØ. Although this exerciser can be run by itself, its full value is not realized unless it is linked to and run with the system exerciser. For information about building a system exerciser to include the TSVØ5 subsystem, refer to DEC/X11 User's Manual, AC-8240Z-MC.

CHAPTER 3
OPERATION

System operations can be divided into various levels or categories of activities. At the most basic level are activities such as powering up and maintaining the system, loading the tape, and performing verification (confidence) checks on system operation. A second category of operating activities involves system generation. When the TSVØ5 is added to the computer system, the software operating system must be modified to include the handler for the tape subsystem. System generation requires building a new copy of the operating system. A third category of operating procedures covers the use of the software utility programs for operations such as copying data from one drive to another, updating files and comparing one file to another. The most complex level of user activity involves designing programs that manipulate the internal workings of the tape subsystem. This chapter devotes sections to these categories of activities.

3.1 ROUTINE OPERATING PROCEDURES

3.1.1 Power Up

On the tape transport front panel, press the power switch to its ON ("1") position. The indicators all light for approximately two seconds and then go out. Then the **UNLOAD** indicator lights and stays on. At this point, the tape unit is ready to be loaded.

3.1.2 Loading Tape

The TSVØ5 loads tape automatically unless the tape is in very bad condition. If you must recover data from a tape that is crumpled or creased on the end, it may be necesssary to load the tape manually. Refer to Appendix B for instructions on manual loading. For best load reliability the beginning of tape leader should be crimped using DEC part number 47-ØØØ38 or equivalent. However, do not repeatedly crimp or remove excessive tape leader as this would cause the BOT marker to be too close to the beginning of tape. Tape crimper part number 47-ØØØ38 can be ordered from the Accessories and Supplies Group, as outlined in Section 3.1.8.2.1.

For normal tape loading, proceed as follows:

1. Ensure that the tape is wound completely onto the reel, and the file protect ring is fully seated, if present on the reel.

NOTE

Most tapes have some form of stick on TAB or rubber block to prevent the tape from unwinding during shipment or storage. These items must be removed so that the tape leader is free to unwind during the auto loading sequence. High levels of static electricity should also be avoided since this could prevent the tape leader from unwinding.

2. Open the front door panel by gently pressing down on the top center of the door. (See Figure 3-1).

3. Hold the tape reel with the file-protect ring side down. Insert the reel into the transport unit, centering it on the hub.

4. Close the door.

CAUTION

Both the tape transport top cover and front panel door are locked when a tape is loaded. Any attempt to force open either the cover or the door before the tape is unloaded will result in mechanical damage to the locking mechanism.

5. Press the LOAD/REWIND switch. This locks the cover and the door, and begins the loading sequence.

6. The LOAD indicator blinks while the tape is being loaded. Typically after 30 seconds, the LOAD indicator stops blinking and remains lighted. This indicates that the tape is loaded and the TSV05 subsystem is ready to use.

7. Press the ON-LINE switch to place the tape subsystem under the control of the host computer. The ON-LINE indicator lights when the TSV05 system is on-line. The ON-LINE switch can be pressed immediately after the load switch.

3.1.3 Rewinding Tape

It is not necessary to rewind the tape during normal operation, as all tape movement is under program control. Under unusual circumstances, however, such as a host system failure or a loss of communications with an upline host, you may wish to rewind the tape under local control. This is done as follows:

1. If the tape subsystem is on-line (indicated by the ON-LINE indicator being on), press the ON-LINE switch once to switch the subsystem off-line.

2. Press the REWIND switch. The LOAD/REWIND indicator blinks while the tape is being rewound, and then remains on continuously when the Beginning-of-Tape (BOT) marker is reached.

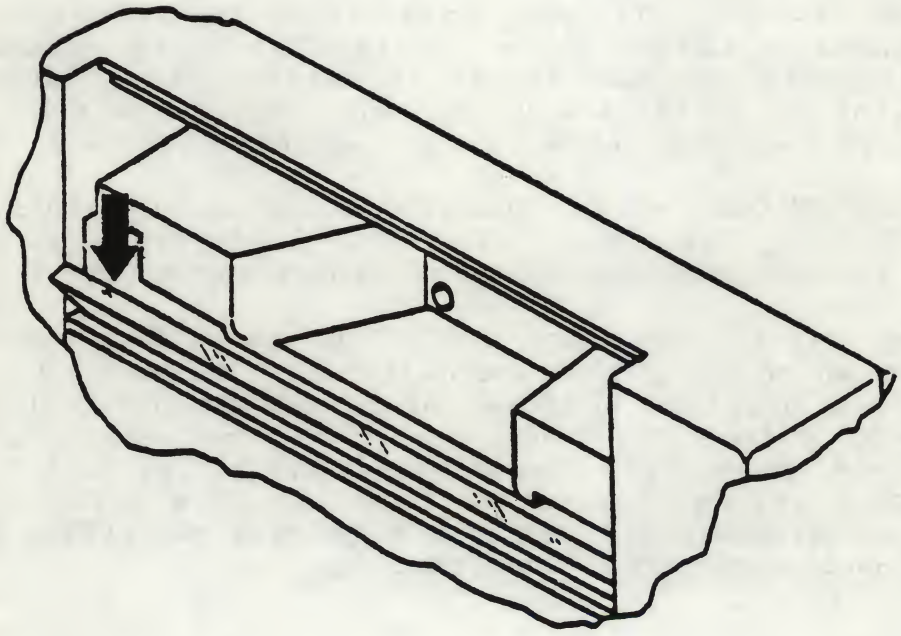


Figure 3-1 Opening the Front Door Panel

3.1.4 Unloading Tape

To unload a tape from the transport, proceed as follows:

1. If a tape subsystem is on-line (indicated by the ON-LINE indicator being on), press the ON-LINE switch once to switch the subsystem off-line.

2. Press the UNLOAD switch. The UNLOAD indicator blinks while the tape is being unloaded. When the unloading process is complete, the UNLOAD indicator lights continuously, and the front panel and top cover are unlocked. A typical unload sequence from BOT takes 15 seconds.

3. Open the front panel door (Figure 3-1) and lift the tape reel out of the tape transport.

4. Close the front panel door.

3.1.5 Restarting the Tape Subsystem

The TSVØ5 ceases operation in the event of a power failure or if it detects a hard operational error.

3.1.5.1 Power Failure -- When line power is interrupted, the transport automatically shuts down and tape motion stops without any physical damage to the tape. When line power is restored, the TSVØ5 powers up in the unload mode. You must press either the LOAD or the UNLOAD switch. If you press the LOAD switch, the LOAD/REWIND indicator blinks while the tape is being reloaded to the BOT marker. When the BOT marker is reached, the LOAD/REWIND indicator remains on continuously, and the ON-LINE switch can be pressed to return the tape subsystem to computer control.

If you press the UNLOAD switch, the UNLOAD indicator blinks while unloading is in progress. When the UNLOAD indicator remains lit continuously, you can open the door and remove the tape.

3.1.5.2 Hard Errors -- When the TSVØ5 encounters an error condition from which it cannot automatically recover, it stops tape movement and displays a series of blinks on the indicators. If this happens, switch the TSVØ5 power off, switch it back on again, and then press the UNLOAD switch. After the UNLOAD indicator stops blinking, remove the tape. At this point, it may be necessary to either call DEC Field Service or refer to the TSVØ5 Magtape Subsystem Pocket Service Guide.

3.1.6 Operator Troubleshooting

It may be possible to avoid a service call by making a few checks before reporting a condition as a problem. If the TSVØ5 is located in an area where several people may be using the tapes and equipment for different purposes, check the following:

1. If the transport does not power up, ensure that the power controller in the TSVØ5 has:

   a. Circuit breaker switches ON.
   b. REMOTE ON/OFF/LOCAL ON switch switched to REMOTE ON.
   c. Remote control cable connected to DEC POWER connector.
   d. Power controller pilot lamp lit.

2. If a tape does not load properly, ensure that:

   a. The tape is in reasonably good condition (if not, refer to manual loading procedure in Appendix B).
   b. Tape has a BOT marker, located per ANSI STDX3.40-1973, 16+ or -2 feet.
   c. Front panel door is completely closed.
   d. The instructions on the loading label are followed.

3. If the subsystem is unable to write a file, ensure that the write enable ring is installed in the tape reel.

4. If intermittent problems occur involving the read/write functions, clean the tape path (see Section 3.1.8 Customer Care).

If it is determined that the equipment is malfunctioning, record the symptoms of the malfunction to aid maintenance personnel in troubleshooting the system.

3.1.7 Confidence Checks

There are three "confidence levels" that can be established by testing. The basic level of confidence is established simply by powering up the system. Both the tape transport and the controller/interface module perform internal self-test programs each time power is applied. Therefore, the ability of the subsystem to power up and load tape establishes that it is probably in good working order.

A second, higher level of confidence can be established by using the console terminal of the host computer sytem to check the status of the TSVØ5 subsystem. This is performed by using the appropriate operating system command to check device status (e.g., on-line or off-line) or to call for a directory listing from a tape mounted in the TSVØ5 system. If the TSVØ5 powers up and loads tape properly, and if the operating system gets directory or status information from the TSVØ5, then the probability that the system is working correctly is very high.

The highest level of confidence in the TSVØ5 is established by running the Data Reliability Diagnostic Program (CVTSEA in the XXDP diagnostic package) and the DEC/X11 exerciser).

3.1.8 Customer Care

The person in charge of the TSVØ5 subsystem is normally responsible for the following tasks:

1. Obtaining operating supplies, including magnetic tape and cleaning supplies.

2. Maintaining the required logs and report files consistently and accurately.

3. Making the documentation available in a location convenient to the system users and maintainers.

4. Ensuring that the exterior of the system and the surrounding area are kept clean.

5. Ensuring that ac plugs are securely plugged in each time the equipment is used.

6. Ensuring that preventive maintainance activities are performed at the suggested periods, or more often if usage and environment warrant.

3.1.8.1 Care of Magnetic Tape -- The person responsible for the TSVØ5 should ensure that system users exercise due care in the handling of magnetic tape. Basic rules of tape care are as follows:

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head. Keeping the tape clean is imperative.

2. Always store tape reels inside containers when the tape is not in use. Keep empty containers tightly closed to guard against dust and dirt.

3. Never touch the portion of tape between the Beginning-of-Tape (BOT) and End-of-Tape (EOT) markers; oil from fingers attracts dust and dirt.

4. Never use a contaminated reel of tape; this spreads dirt to the clean tape reels and could adversely affect tape transport reliability.

5. Always handle tape reels by the hub hole; squeezing the reel flanges leads to tape edge damage when winding or unwinding tapes.

6. Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.

7. Do not place magnetic tape near line printers or other devices that produce paper dust.

8. Do not place magnetic tape on top of the tape transport or in any other location where it may be affected by hot air.

9. Do not store magnetic tape near electric motors.

3.1.8.2 Preventive Maintenance -- The tape transport is a highly reliable precision instrument that provides years of trouble-free performance when properly maintained. For optimum performance and reliability, a planned and scheduled program of routine inspection and maintenance is essential. Preventive maintenance consists of cleaning only a few items, but the cleanliness of these items is essential to proper tape transport operation. The frequency of maintenance operations will vary with the environment and the degree to which the transport is used. Therefore, a rigid schedule for all machines is difficult to define. Cleaning after every eight hours of operation is recommended for units in constant operation in ordinary environments. This schedule should be modified if experience shows other periods are more suitable. Typically, new tapes or tapes near the end of their life will produce the most oxide buildup within the transport and require more frequent cleaning. Table 3-1 shows the recommended frequency of maintenance activities. The replacement of filters, reel motors and head wear check is to be performed by DEC Field Service personnel. The other activities are to be performed by the customer.

Before performing any cleaning operation, remove the supply reel and store it properly. When cleaning, be gentle but thorough.

Table 3-1 Suggested Preventive Maintenance

Maintenance Operation	Frequency	Quantity to Maintain
Clean Head, Guides, Roller Guides, Tape Path	Once per shift	-
Clean Tape Cleaner	Once per shift	1
Clean Reel-Hub Pads	Once per shift	3
Clean Tachometer Roller	Once per week	1
Check Head Wear	2,500 Hours	1
Replace Reel Motors	10,000 Hours	2
Check Air Filter	Every 3 Months	1

3.1.8.2.1 Magnetic Tape Transport Cleaning Kit -- A magnetic tape transport cleaning kit (TUC02, Part Number 220012) has been carefully assembled to provide materials that will not harm tape equipment or leave any residue to interfere with data reliability. The hints contained in the following paragraphs will help you obtain the very best results from the kit.

WARNING

When using DECmagtape cleaning fluid, avoid excessive skin contact and contact with the eyes. Do not swallow it. Use the cleaning fluid only in a well ventilated area.

When cleaning tape equipment, never dip a dirty cleaning swab or wipe into the can.

Always keep the can of fluid tightly closed when not in use; the fluid evaporates rapidly when exposed to air.

CAUTION

Do not use acetone, lacquer thinner or rubbing alcohol to clean the tape path and related parts.

Should you encounter any unusually stubborn dirt deposit that resists the cleaner, try a mild soap and water solution to dislodge it. After using soap, be sure to wash down the affected area thoroughly with cleaning fluid to remove soapy residue.

If you need more cleaning materials, tape crimper Part Number 47-00038, or other items, forward orders for supplies, accessories or documentation to:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

Contact your local sales office or call DIGITAL Direct Catalog Sales toll-free 800-258-1710 from 8:30 a.m. to 5:00 p.m. Eastern Standard Time (U.S. customers only). New Hampshire customers should dial (603) 884-6660. Terms and conditions include net 30 days and F.O.B. DIGITAL plant. Freight charges will be prepaid by DIGITAL and added to the invoice. Minimum order is $35.00. Minimum does not apply when full payment is submitted with an order. Checks and money orders should be made out to Digital Equipment Corporation.

3.1.8.2.2 **Accessing the Tape Path Area** -- Refer to Figure 3-2. Raise the cabinet top cover by grasping the handle on the top cover and lifting. When the top cover is raised far enough, the support arm latches to keep the cover up.

Raise the top cover of the tape transport unit by reaching in through the front panel door and pressing upward at the front area of the top cover.

3.1.8.2.3 **Cleaning the Tape Path and Related Parts** -- Refer to Figure 3-3. Using foam-tipped swabs soaked in cleaning fluid, gently wipe the following parts:

1. Read/Write head
2. Tachometer roller

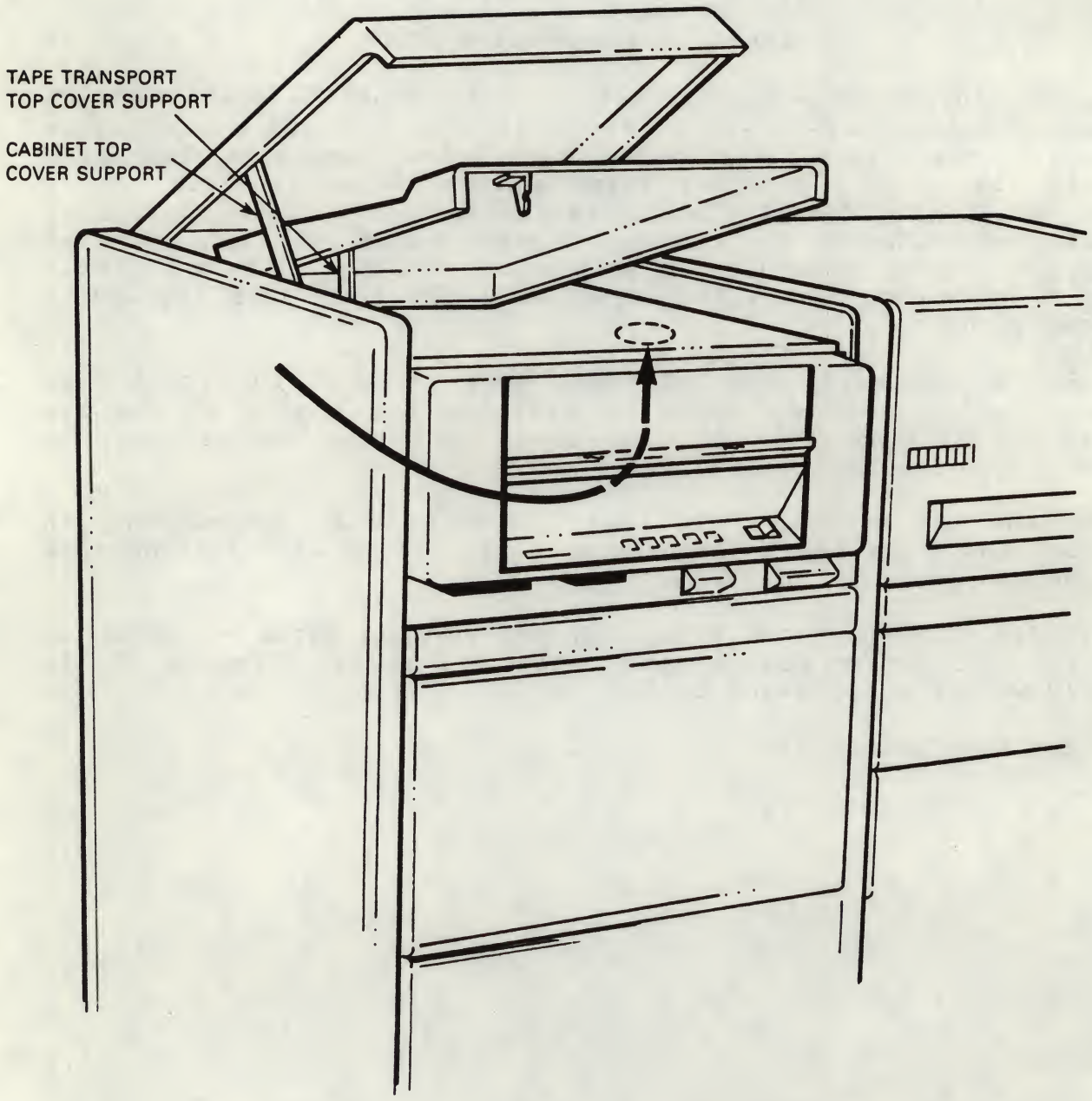


Figure 3-2 Accessing the Tape Path Area

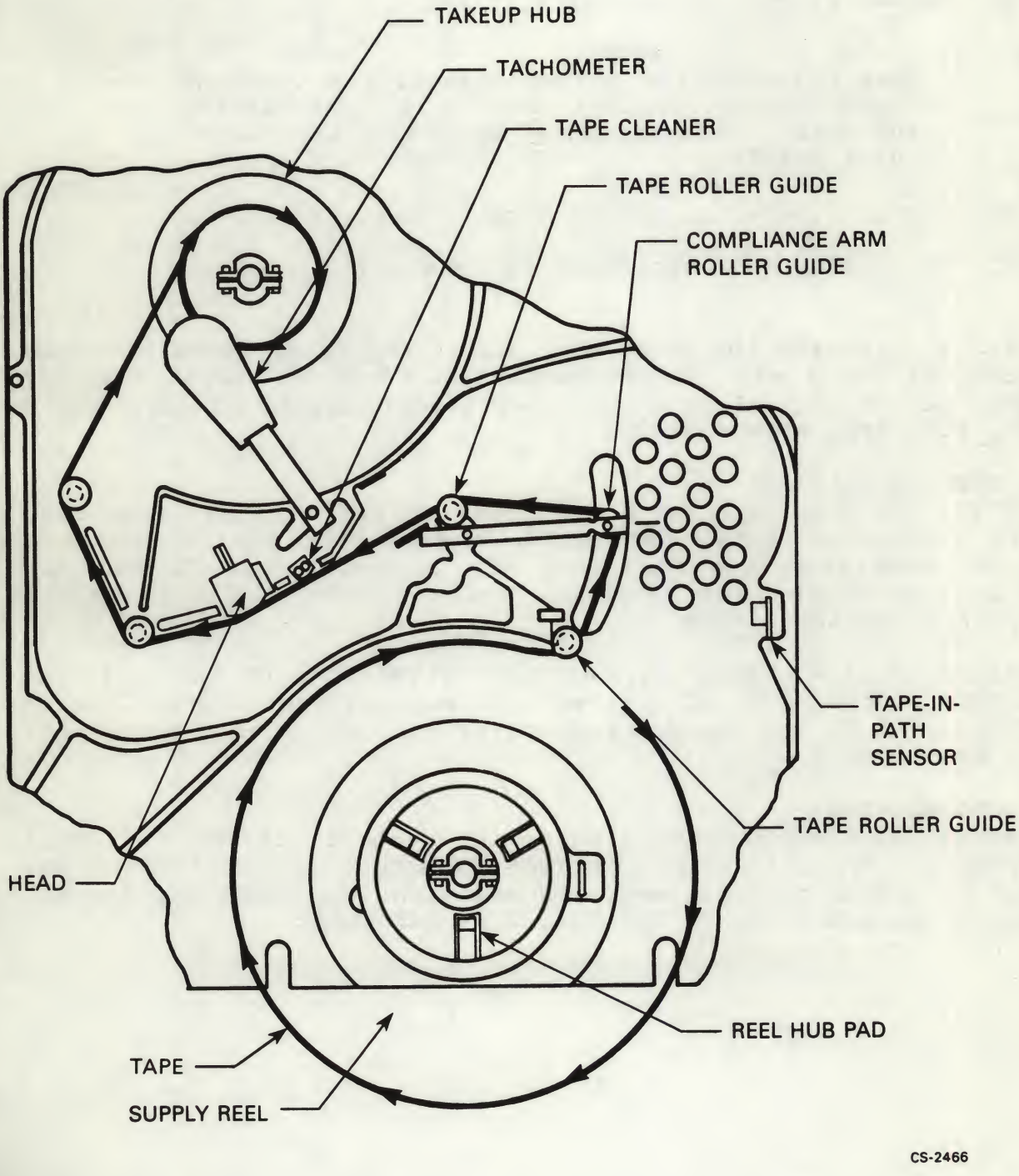


Figure 3-3 Tape Path and Related Parts

3. Tape Cleaner.

CAUTION

Exercise care to avoid damage to the sharp edges of the blades on the tape cleaner.

4. Roller guides (quantity of five).

NOTE

When cleaning the roller guides, the cleaning fluid should contact only the tape-bearing surfaces. This prevents degreasing the roller guide bearing.

5. Supply hub pawls (quantity of three).

6. Tape path. (use the supplied texwipes).

3.1.8.2.4 **Cleaning the Housing** -- Clean the front panel door and the control panel with Miller Stephenson Chemical Company MS-260, Windex, or an equivalent commercial grade plastic cleaner and a clean, lint-free wipe material.

3.2 TSV05 OPERATIONS

The TSV05 is compatible with TS11/TS04 software in all operating system level functions. Generally, any utility that supports a magtape subsystem (device code MS) supports the TSV05. For detailed procedures and examples, refer to the utilities manual for your operating system.

Operation of the TSV05 may differ slightly from that of the TS11/TS04 at the level of user-written application programs. Refer to Section 3.3. for detailed descriptions of program-accessible TSV05 functions.

3.3 PROGRAMMING

The TSV05 follows the same programming protocol as the TS11/TS04 subsystem. The nature of the TS05 transport dictates that some status bits will be redefined. In addition, the TSV05 has special features not available in the TS11/TS04 subsystem.

3.3.1. Overview

The functions listed in Table 3-2 make up the TSV05 Subsystem Command Set. These commands utilize "command packets" stored in the computer system memory to operate the transport and transfer data. Some commands have various sub-commands, termed "modes". The interface device registers are used to initiate command packet processing and retrieve basic status. This section describes register manipulation and provides an overview of packet protocol (the format used to transfer commands and data). A detailed description of the commands is provided in Section 3.3.4.

The TSV05 has four device registers which occupy only two LSI-11 Bus word locations: a Data Buffer (TSDB), a Bus Address Register (TSBA), a Status Register (TSSR) and an Extended Data Buffer (TSDBX). The TSDB is an 18-bit register that is parallel loaded from the LSI-11 Bus or from the TSV05 controller (M7196) itself. A 16-bit portion of this register is used as a word buffer register; it is written into by the CPU to initiate and operate, and it is written into by the controller logic itself to store data to be transmitted to LSI-11 Bus memory during a DMA cycle. The TSDB can be loaded from the LSI-11 Bus by three different transfers from the CPU. Two transfers are for maintenance purposes (byte transfer, and DATOB at high byte or low byte), and the third is for the normal (word) operation (DATO) to initiate an operation. This register is write-only and is not cleared at power on, subsystem initialize or bus initialize. This register can be loaded without the tape transport connected, since all controller functions reside within the M7196 interface module.

Table 3-2 TSVØ5 Assigned Command Modes

Command Name	Mode Name/Description
GET STATUS	Get Status (update the Extended Status registers in the message buffer in memory)
READ	Read Next (Forward) Read Previous (Reverse) Reread Previous (Space Reverse, Read Forward) Reread Next (Space Forward, Read Reverse)
WRITE CHARACTERISTICS	Load Message Buffer Address and Set Device Characteristics
WRITE	Write Data Write Data Retry (Space Reverse, Erase, Write Data)
POSITION	Space Records Forward Space Records Reverse Skip Tape Marks Forward Skip Tape Marks Reverse Rewind
FORMAT	Write Tape Mark Erase Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)
CONTROL	Message Buffer Release Rewind and Unload Clean Tape (handled as a NO-OP) Rewind with Immediate Interrupt *
INITIALIZE	Controller/Drive Initialize
WRITE SUBSYSTEM MEMORY	Diagnostic function. Allows test sequences and data patterns to be entered into the controller.

* Extended function, not part of the TS11/TSØ4 repertoire.

Commands are not written to the TSVØ5 LSI-11 Bus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB register. The command pointer is used in the TSVØ5 subsystem to retrieve words in memory called the Command Packet. The words in the Command Packet instruct the system as to the function to be performed. These words contain any function parameters such as bus address, byte count, record count, and modifier flags.

The TSBA is an 18-bit register (22-bits when the high byte of the TSSR is written to) that is parallel loaded from the TSDB every time the TSDB is loaded. TSDB bits 15-2 load into TSBA bits 15-2, TSDB bits 1 and Ø load into TSBA bits 17 and 16, and zeros are loaded into TSBA bits 1 and Ø (thereby specifying a modulo-4 address). TSBA bits 17 and 16 are displayed in TSSR bits 9 and 8, respectively. (TSDB can be extended to 22 bits by firstloading TSDB bits 18-22 into the high byte of TSSR. The Extended Features Switch must be ON or else bits 18-22 are ignored). The TSBA register is incremented or decremented by two for DMA word transfers, or by one for DMA byte transfers. The two major purposes of the TSBA register are as follows:

1. The TSBA can be used as a command pointer, pointing to the "functional device registers" (command and message buffers). These are located somewhere in LSI-11 Bus address space. The contents loaded into the TSDB when the TSVØ5 is the bus slave is considered the command pointer. In this mode, the TSVØ5 receives data (command buffer words) and stores them internally on the M7196 module for storage and/or execution.

2. The TSBA can be used as a data pointer (bus address for DMA), pointing to data buffer areas located somewhere in the LSI-11 Bus address space. In this mode, the controller loads TSBA with data pointer information from internal storage. The contents are then used to point to data buffer areas while transferring Tape data between CPU memory and the tape transport. The data pointer is extended to 22 bits (18-21 are zeros) if the TSSR high byte is not first loaded, or if the Extended Features Switch is OFF.

The TSSR is a #16-bit register that can be updated only from the M7196 internal logic. It cannot be modified from the LSI-11 Bus. In this register, major system status can be observed.

The tape transport, when on-line, is under control of the microprocessor and related microcode within the M7196 interface/controller module. When the transport is off-line, the transport is under control of its own internal logic, which can in turn be controlled by the operator using switches on the front panel.

Before the TSVØ5 begins a function, the LSI-11 must assemble a command packet in main memory. The command packet is always four words long, although not all commands use all four of the words in the packet. The words in the command packet may be thought of as the contents of several registers:

1. Command Register (CMDR)

2. Data Pointer Register (DPR)

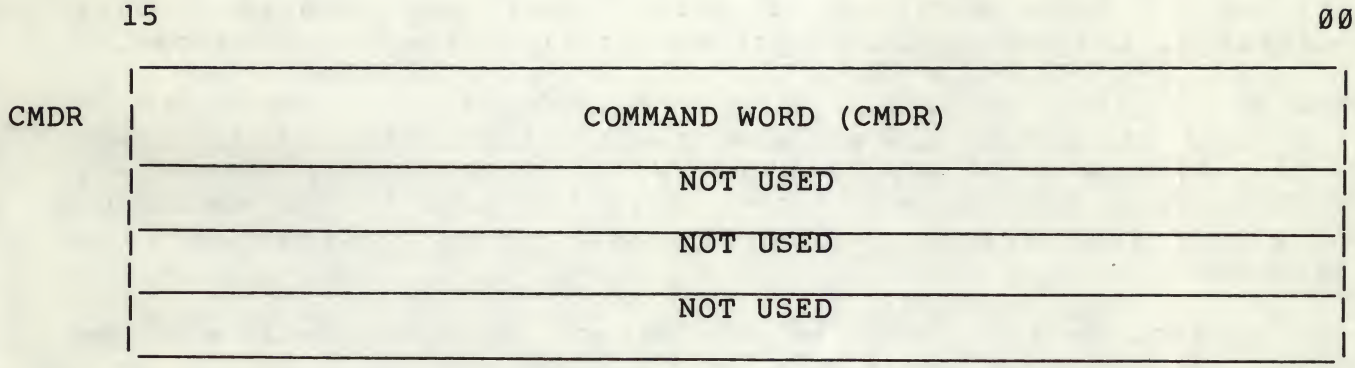
3. Positive Byte Count Register (BPCR)

The Command Register (CMDR) contains the machine language representation of one of the commands listed in Table 3-2. The Data Pointer Register (DPR) contains the address of the data to be manipulated. The DPR consists of two words: a low-order address word containing bits 15-ØØ, and a high-order address word containing either bits 17-16 (for 18-bit addressing) or bits 21-16 (for 22-bit addressing). In the 18-bit addressing mode, bits Ø1-ØØ of the DPR high-order address word are used to specify bits 17-16 of the address. If the extended features switch is on, the 22-bit addressing mode can be used.

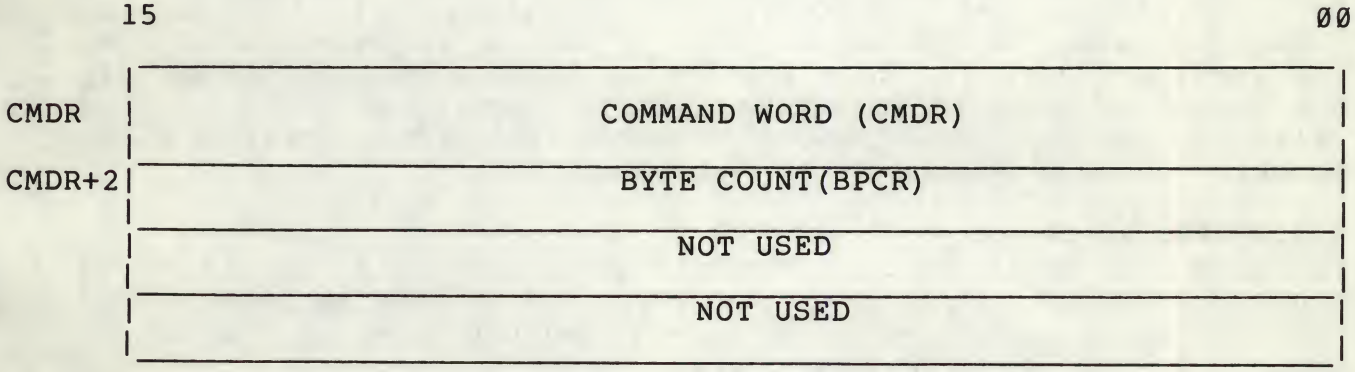
In this case, bits Ø5-ØØ of the DPR high-order address word are used to specify address bits 21-16.

When the command being used does not involve a data operation, the two DPR words are not used in the command packet (see Figure 3-4).

A. One-word type



B. Two-word Type



C. Four-word Type

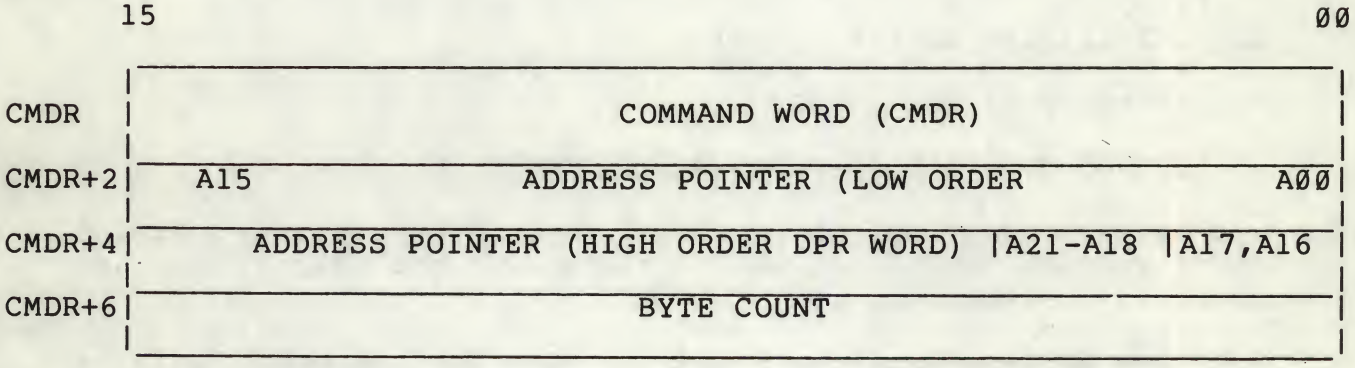


Figure 3-4 Command Packet Types

The Positive Byte Count Register (BPCR) contains the number of items to be manipulated during the operation specified by the command. In a packet that includes DPR words, the BPCR word follows the DPR word. If a packet does not involve a data operation, the BPCR word, if present, follows the command words.

Message packets are issued by the M7196 controller and built in the host CPU memory space. Subsystem operation requires a message buffer address to be supplied on a Write Characteristics command. This command must be the first command issued to the subsystem after an initialize. Otherwise, all other commands will be rejected.

The command pointer must be an address on a modulo-4 boundary (i.e., beginning at octal Ø, 4, 1Ø, 14, etc.).

The DPR is eventually loaded into TSBA to be used as the LSI-11 Bus address for DMA transfers. The BPCR is used to indicate the number of bytes (8 bits of data per byte) to be moved to or from the transport during a data transfer. It is also used to specify the number of records in a Space Record command or the number of files in a Skip Tape Marks command. The CMDR specifies the function to be executed by the subsystem.

3.3.2 Registers

The TSVØ5 contains four hardware device registers on the M7196 controller module, and also five "remote" device registers that the controller maintains in a Message Buffer area of the LSI-11 memory. The hardware registers are:

1. LSI-11 Bus Address Register (TSBA).
2. LSI-11 Data Buffer (TSDB).
3. Status Register (TSSR).
4. Extended Data Buffer Register (TSDBX).

The remote registers set up in LSI-11 memory are Extended Status Registers Ø-4 (XSTØ-4). Register formats and bit definitions are presented in the sections that follow.

3.3.2.1 Bus Address Register (TSBA) -- The Bus Address Register (TSBA) is a Read-Only hardware register located at the first I/O register address. In normal operating mode, it displays the low-order 16 bits of the memory address to be used or being used by the controller to access system main memory (e.g., for command buffer fetch, message buffer store, or data transfer). In Maintenance Mode, it displays data from the Wraparound tests invoked by writing into TSDB. Figure 3-5 illustrates the TSBA, and Table 3-3 defines the bits.

LSI-11 Bus Address + Ø -- Read-Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
A15	A14	A13	A12	A11	A10	AØ9	AØ8	AØ7	AØ6	AØ5	AØ4	A13	AØ2	AØ1	AØØ
S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S

Figure 3-5 TSBA Register Format

Table 3-3 TSBA Register Bit Definitions

Bit	Name	Definition
15	A15	Bus address bit 15
14	A14	Bus address bit 14
13	A13	Bus address bit 13
12	A12	Bus address bit 12
11	A11	Bus address bit 11
10	A10	Bus address bit 10
Ø9	AØ9	Bus address bit Ø9
Ø8	AØ8	Bus address bit Ø8
Ø7	AØ7	Bus address bit Ø7
Ø6	AØ6	Bus address bit Ø6
Ø5	AØ5	Bus address bit Ø5
Ø4	AØ4	Bus address bit Ø4
Ø3	AØ3	Bus address bit Ø3
Ø2	AØ2	Bus address bit Ø2
Ø1	AØ1	Bus address bit Ø1
ØØ	AØØ	Bus address bit ØØ

Address Bits 15 through ØØ normally reflect the low-order 16 bits of the 22-bit address used by the controller to access LSI-11 Bus memory. They can be loaded by:

1. The CPU when writing a word into TSDB, to define the address of the Command Buffer for the next operation. TSDB<15:Ø2> are copied into TSBA<15:Ø2>, and TSBA<Ø1:ØØ> are set to Ø.

2. The CPU writing into the high byte (DATOB) of TSDB (for a maintenance function). TSDB bits 15-Ø8 are copied into both bytes of TSBA. Data for bits Ø7-ØØ is TSDB<15:Ø8>. TSDB bits Ø8 and Ø9 are copied into TSSR bits Ø8 & Ø9 (A16, A17).

3. The CPU writing into the low byte (DATOB) of TSDB (for a maintenance function). TSDB bits 07-00 are copied to TSBA<07:00>. TSBA <15:08> is then loaded from TSDB bits 07-00.

4. The CPU writing a word (DATO) into TSDB in Maintenance Mode. (Maintenance mode is achieved as a result of b or c).

5. The controller, for specifying bits 15-00 of a DMA address. TSBA is not modified by Initialize.

3.3.2.2 **Data Buffer Register (TSDB)** -- The TSDB is, externally, a 16-bit Write-Only register that is parallel loaded from the LSI-11 Bus. Internally, it is a 22-bit register. It can be loaded from the CPU by four different types of transfers. Two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte); these place the controller into Maintenance Mode, which can be cleared only by an Initialize, and causes the internal "Data Wraparound" functions. The third is for maintenance purposes (DATO word when in Maintanance Mode). The fourth is for normal operation (DATO word when not in Maintenance Mode) to specify a Command Pointer. The 4-bit extension to TSDB is written at the high byte of the TSSR location. These address bits are ignored if the Extended Features Switch is OFF. The extension is cleared after it issued once and so must be reloaded if extended addressing is to be used on subsequent command pointers. (It must be loaded before the TSDB is loaded.) It is also cleared by Initialize.

The controller will respond whenever the TSDB location is written to, but will be loaded only when the SSR bit in the TSSR register is set (if SSR is clear, the RMR bit in TSSR will be set). Writing into TSDB clears SSR. After a DATO or DATOB to TSDB (for maintenance data "wraparound"), SSR momentarily clears then sets when the data "wraparound" has been performed. An Initialize should be performed (i.e., write into TSSR) in order to use the controller again for normal operation. Note that entering Maintenance Mode (by performing a DATOB to either byte of the TSDB) causes the NBA (Need Buffer Address) bit in TSSR to be set and automatic running of the idle-time On-Line Microdiagnostics to be inhibited.

The TSDB register is illustrated in Figure 3-6 and the bits are listed and defined in Table 3-4.

LSI-11 Bus Address + Ø -- Write-Only

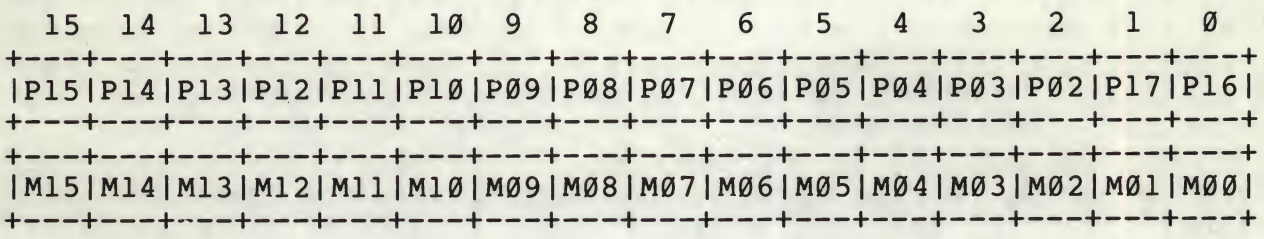


Figure 3-6 TSDB Register Format

Table 3-4 TSDB Register Bit Definitions

Bit	Name	Definition
15-02 01-00	P<15:02> P<17:16> (DATO Word, Normal Mode)	Command Pointer bits 17-02. When the TSDB is written as a word, and SSR=1, and the controller is not in Maintenance Mode, the data is loaded into bits 17-02 of both the TSBA Output File register (for reading onto the LSI-11 Bus) and into an internal TSBA register and command processing commences. TSBA bits 01-00 are cleared to 0 (modulo-4 address). In addition, the Extended TSDB Register (TSDBX) is loaded into TSBA bits 21-18; TSDBX must be loaded before TSDB.
15-08	M<15:08> (DATOB to High Byte)	Maintenance Data bits 15-08 for wraparound to TSBA. If the wraparound is correct, M<15:08> appears in both bytes of TSBA. A DATOB to TSDB places the controller into maintenance mode.
07-00	M<07:00> (DATOB to Low Byte)	Maintenance Data bits 07-00 for wraparound to TSBA. If the wraparound is correct, M<07:00> appears in both TSBA<07:00> and in TSBA<15:08> .A DATOB to TSDB places the controller into maintenance mode.
15-00	M<15:00> (DATO) Word in Maint. Mode)	Maintenance Data bits 15-00. This function can be in used for specifying the address used in the Low-Byte Data Wrap test. Bits 15-12 are reserved for future maintenance functions and should be written to 0.

3.3.2.3 Status Register (TSSR) -- TSSR is a 16-bit register. Although defined as a Read/Write register, its contents cannot be directly modified by the LSI-11 Bus. It can be read to examine status, but writing into it causes a hardware initialize of the controller. (A DATOB) to the high byte only of the TSSR, however, loads the extended TSDBX). The contents of the register is modified by the M7196 controller. The register format is illustrated in Figure 3-7. Table 3-5 gives the register bit definitions. If the initialize diagnostic fails, this register has alternate bit definitions.

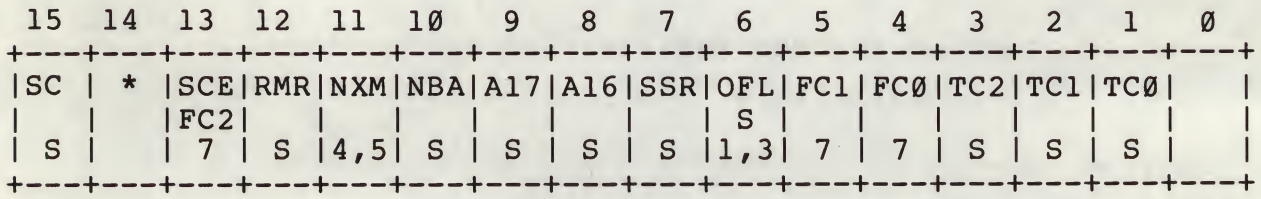


Figure 3-7 TSSR Register

Table 3-5 TSSR Register Bit Definitions

Bit	Name	Code	Definition
15	SC	S	Special Condition - When set, indicates that the last command was not completed without incident: either an error was detected or an exception condition (i.e., Tape Mark on read, reverse motion at BOT, etc.) occurred. Also set by the error bits in TSSR: RMR, and NXM. Indicates that the Termination Class bits are nonzero (unless RMR is the only error - see RMR). Cleared by Initialize unless a self-test error is detected, in which case SC is set.
14	*	--	Not used in TSVØS, UPE in TS11.
13	SCE	FC2 7	Sanity Check Error. Set when the controller detects an internal failure. This is considered serious enough that a Message Buffer is not sent out. SPE in TS11.

Table 3-5 TSSR Register Bit Definitions (Cont)

Bit	Name	Code	Definition
12	RMR	S	Register Modification Refused - Set when the TSDB is written from the LSI-11 Bus and SubSystem Ready (SSR) is not set. Causes the Special Condition (SC) bit to be set but no Termination Class (the TSV05 never sees the data written) because on a system with no bugs, RMR can be set if TSDB is written while an ATTN message is being output. If ATTN's are not enabled, RMR setting indicates a fatal controller problem or a software bug.
11	NXM	4,5	Nonexistent Memory - Set when trying to do a DMA transfer to/from a memory location which does not exist (does not respond within 12 usec). May occur when fetching a Command Packet, fetching or storing data, or storing the Message Packet.
10	NBA	S	Need Buffer Address - When set, indicates that the TSV05 needs a Message Buffer address. Set by Initialize and performing a DATOB to the TSDB (i.e., to enter Maintenance Mode). Cleared during the Write Characteristics command (if a valid address was given). If NBA=1 and any command other than Write Characteristics is given, the operation is terminated with Function Reject.
09-08	A<17:16>	S	Address Bits 17-16. A17 and A16 display bits 17 and 16 of the internal TSBA register, which holds a Command Pointer or DMA address. Loaded from TSDB bits 01-00 when TSDB is written.

Table 3-5 TSSR Register Bit Definitions (Cont)

Bit	Name	Code	Definition
Ø7	SSR	S	Sub-System Ready - When set, indicates that the TSVØ5 is not busy and is ready to accept a new command pointer. Cleared by writing the TSDB. Also cleared by Initialize, then set by the controller if the basic microdiagnostics are successfully passed.
Ø6	OFL	S 1,3	Off Line - When set, indicates that the TSØ5 transport is off-line and unavailable for any tape motion commands. This bit can cause a Termination Class of 1 (on an ATTN interrupt) or 3 (results in Non-Executable Function, NEF, status). This bit does not indicate the current status of the Tape Transport (updated on command completions).
Ø5-Ø4	FC<1:Ø>	7	Fatal Termination Class Code - Used to indicate the type of fatal error which has occurred on the TSVØ5. The code is valid only when the SC bit is set and the Termination Class Code (TC) bits are all set (111); they are clear otherwise. The FC codes are: Code Meaning Ø Internal diagnostic failure. See the Error Code byte (XST3) for the failed function. Initialize must be issued for the controller to accept further commands. 1 Reserved. 2 Not used. 3 Reserved for detection of power down on transport (not currently implemented).

Table 3-5 TSSR Register Bit Definitions (Cont)

Bit	Name	Code	Definition
Ø3-Ø1	TC<2:Ø>	S	Termination Class Code - This 3-bit field acts as a word offset value whenever an error or exception condition occurs on a command. Each of the 8 possible values of this field represents a particular class of errors or exceptions. The conditions in each class have similiar significance and recovery procedures (as applicable). The codes are: Code Meaning Ø Normal Termination 1 Attention Condition 2 Tape Status Alert 3 Function Reject 4 Recoverable Error - tape position is one record down tape from start of function. 5 Recoverable Error - tape not moved 6 Unrecoverable Error - tape position lost 7 Fatal Controller Error - (See Fatal Class Codes)
Ø	-	-	Not Used

3.3.2.4 Extended Data Buffer Register (TSDBX) -- The Extended Data Buffer Register (TSDBX) is a Write-Only hardware byte register located at the fourth byte address of the TSVØ5 I/O register block. This address corresponds to the high-order byte of the TSSR register. The TSDBX is used to specify the most significant four bits of a 22-bit command pointer address, and also to allow an automatic tape boot sequence to be performed. TSDBX can be written only by a byte-access (DATOB) cycle addressed to the high byte of TSSR. If the Extended Features switch is Off when TSDBX is written, only the boot bit is examined; the other bits are ignored.

Figure 3-8 illustrates the format of TSDBX, and Table 3-6 describes each bit.

Assume the Extended Features switch is on. Once written, the contents of the least-significant four bits of TSDBX are transferred to bits 18 through 21 of the internal TSBA (Bus Address) register for use as a command pointer. The low order 18 bits of the command pointer are specified by writing into the TSDB register, which starts operation and then clears TSDBX. Therefore, a subsequent load of only the TSDB will specify a 22-bit command pointer address with the high-order four bits equal to zero. For the TSDBX register to be properly written, the SSR (Subsystem Ready) bit in TSSR must be set; if it is not, the RMR (Register Modification Refused) bit will be set and no modification to TSDBX will occur. When the TSDBX is written, the SSR bit is not cleared. Therefore, RMR should be checked for, before TSDB is written. Writing the TSDB will begin processing on TSDBX. If the Boot bit is not set, the command pointed to by the 22-bit TSDB will be retreived, and command processing will begin. If the Boot bit is set, SSR will remain clear until the boot sequence is complete or until an error occurs.

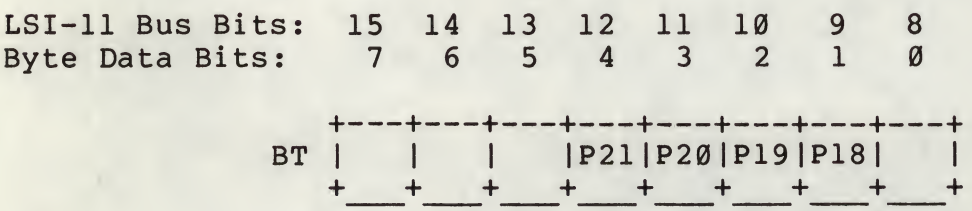


Figure 3-8 TSDBX Register Format

Table 3-6 TSDBX Register Bit Definitions

Bit	Name	Definition
15	BT	Boot Command Bit. When written to 1, with SSR=1, causes the tape to be rewound to BOT, the first tape record to be skipped, and the second record (only the first 512 bytes of it) to be loaded into CPU memory space starting at location Ø.
14-12	-	Reserved. Should always be written to Ø.
11-Ø8	P<21:18>	Command Pointer bits 21-18. When the TSDBX is written, and SSR=1, the data is loaded into bits 21-18 of the internal TSBA register. TSDBX is cleared after TSDB is written and is also cleared by Initialize.

3.3.2.5 Extended Status Register Ø (XSTØ) -- Extended Status Register Ø (XSTØ) appears as the fourth word in the Message Buffer stored by the TSVØ5 upon completion of a command or on an Attention (ATTN). Figure 3-9 illustrates the register format and Table 3-7 describes each bit.

15	14	13	12	11	1Ø	9	8	7	6	5	4	3	2	1	Ø
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT
									S						
S,2	2	2	2	3,6	3	3	3	S	1,3	S	S,3	S	S,3	S,3	S,2

Figure 3-9 XSTØ Register Format

Table 3-7 XSTØ Register Bit Definitions

Bit	Name	Code	Description
15	TMK	S,2	Tape Mark Detected. Set whenever a Tape Mark is detected during a Read, Space, or Skip command, and also as a result of the Write Tape Mark or Write Tape Mark Retry commands.
14	RLS	2	Record Length Short. This bit indicates that either the record length was shorter than the byte count on Read operations, a Space Record operation encountered a tape mark or BOT before the position count was exhausted, or a Skip Tape Marks command was terminated by encountering BOT or a double tape mark (if that operational mode is enabled, see LET) prior to exhausting the position counter.
13	LET	2	Logical End of Tape. Set only on the Skip Tape Marks command when either two contiguous tape marks are detected, or when moving off of BOT and the first record encountered is a tape mark. The setting of this bit does not occur unless this mode of termination is enabled through use of the Write Characteristics command.
12	RLL	2	Record Length Long. When set, indicates that the record read on a Read was longer than the byte count specified.
11	WLE	3,6	Write Lock Error. When set, indicates that a write operation was issued but the mounted tape did not contain a write enable ring.
1Ø	NEF	3	Non-Executable Function. When set, indicates that a command could not be executed due to one of the following conditions: - The command specified reverse tape direction but the tape was already at BOT. - The issuing of any motion command when the Volume Check bit is set. - Any command, except Get Status or Drive Initialize, when the transport is off-line - Any write command when the tape does not contain a write enable ring (also causes Write Lock Status - WLE)

Table 3-7 XSTØ Register Bit Definitions (Cont)

Bit	Name	Code	Description
Ø9	ILC	3	Illegal Command. Set when a command is issued and either its Command field or its Command Mode field contains codes which are not supported by the TSVØ5.
Ø8	ILA	3	Illegal Address. Set when a command specifies an address more than 18 bits (when the Extended Features switch is off) or more than 22 bits (when the Extended Features switch is on), or an odd address when an even one is required.
Ø7	MOT	S	Motion. Tape is moving. Indicates that the transport is asserting Formatter Busy or Rewinding status.
Ø6	ONL	S	On Line. When set, indicates that the TSØ5 transport is on-line and operable. A change in this bit can cause a Termination Class of 1 (ATTN interrupt, if ATTENTIONS are enabled). If ONL is clear and a motion command is issued, causes NEF (Termination Class 3).
Ø5	IE	S	Interrupt Enable. Reflects the state of the Interrupt Enable bit supplied on the last command.
Ø4	VCK	S	Volume Check. When set, indicates that the transport has been either powered down or turned off-line. Cleared by the Clear Volume Check (CVC) bit in the Command Header word. This bit can cause a Termination Class of 3.
Ø3	PED	S	Phase-Encoded Drive. Always Set. Indicates that the TSVØ5 is capable of reading and writing only phase encoded data.
Ø2	WLK	S,3	Write Locked. When set, indicates that the mounted reel of tape does not have a write enable ring installed. The tape is, therefore, write protected.
Ø1	BOT	S,3	Beginning of Tape. When set, indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape.

Table 3-7 XSTØ Register Bit Definitions (Cont)

Bit	Name	Code	Description
ØØ	EOT	S,2	End of Tape. This bit is set whenever the tape is positioned at or beyond the End of Tape reflective strip. Does not reset until the tape passes over the strip in the reverse direction under program control. If the controller is read buffering (pre-reading records from tape automatically) and the EOT strip is seen, this bit will not be set until the program actually requests the record associated with the EOT.

3.3.2.6 Extended Status Register 1 (XST1) -- Extended Status Register 1 (XST1) appears as the fifth word in the Message Buffer stored by the TSVØ5 upon completion of a command or on an Attention (ATTN). Figure 3-1Ø illustrates the register format and Table 3-8 describes each bit.

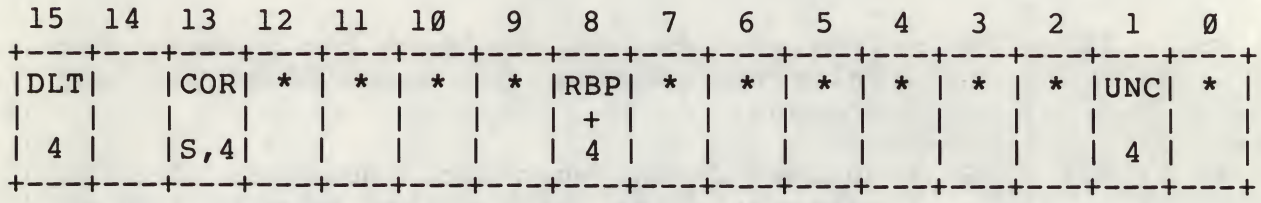


Figure 3-1Ø XST1 Register Format

Table 3-8 XST1 Register Bit Definitions

Bit	Name	Code	Description
15	DLT	4	Data Late. Set when the M7196 internal FIFO buffer is full on a Read and the transport attempts to enter another byte, or when it is empty on a Write and the transport requests another byte. These conditions occur whenever the LSI-11 Bus latency exceeds the required data transfer rate of the TSØ5.
14	-	-	Not Used.
13	COR	S,4	Correctable Data. When set, indicates that a correctable data error has been encountered while reading or writing. On a Write, this bit causes a termination class of 4. On a Read, the termination class is Ø (no corrective action required).
12-9, 7-2, Ø	-	-	Not used by the TSVØ5; always set to Ø. In the TS11, these bits indicate Crease Detected (CRS), Trash in Gap (TIG), Deskew Buffer Fail (DBF), Speed Check (SCK), Invalid er Fail (DBF), Speed Check (SCK), Invalid Preamble or Postamble (IPR, IPO), Sync Failure (SYN), Invalid End Data (IED), Postamble Short or Long (POS, POL), and Multi-Track Error (MTE). The TSØ5 transport reports any of these errors as Hard Error, causing the UNC bit (bit 1) to be set.
8	RBP	4	Read Bus Parity Error. Set when the controller detects a parity error on the Read Data lines of the transport bus (during a Read or Write). If this parity error was also detected by the transport, the UNC bit will also be set. The problem is most likely in the bus drivers in the transport, the bus receivers in the controller, or in the transport bus cable.

Table 3-8 XST1 Register Bit Definitions (Cont)

Bit	Name	Code	Definitions
1	UNC	4	Uncorrectable Data or Hard Error. Set, in response to the transport asserting Hard Error, during a read or write to indicate that one of the following has occurred: - False preamble detection - False postamble detection - Multichannel dropout - Parity error without associated channel dropouts (could result from bad Write Data interface circuit in the controller) - Loss of data envelope prior to postamble detection - Excessive skew

3.3.2.7 **Extended Status Register 2 (XST2)** -- Extended Status Register 2 (XST2) appears as the sixth word in the Message Buffer stored by the TSVØ5 upon completion of a command or on an Attention (ATTN). Figure 3-11 illustrates the register format and Table 3-9 describes each bit. Note that the low-order 8 bits of this register have special meaning for the Write Characteristics command; unlike the TS11, there is no display of dead tracks, or residual capstan tick count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
OPM	RCE	*	*		WCF		*	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RLØ
	@							@	@	@	@	@	@	@	@
S	7F2				7			S	S	S	S	S	S	S	S

Figure 3-11 XST2 Register Format

Table 3-9 XST2 Register Bit Definitions

Bit	Name	Code	Description
15	OPM	S	Operation in Progress. (Tape Moving)
14	RCE	@	RAM Checksum Error. Set on a Read or Write when the checksum of a data block extracted from the M7196 internal RAM does not match the checksum computed when the data was entered. Causes Fatal termination. This Bit is (SIP) Silo parity in the TS11.
13, 12, 8	-	*	Not used by the TSV05; always set to 0. In the TS11, bit 13 is Serial Bus Parity at Drive, bit 12 is Capstan Acceleration Fail, and bit 8 is Parity Dead Track.
11,9	-	-	Not used.
10	WCF	7	Write Clock Failure. Set during a write to indicate that the M7196 internal FIFO buffer is not being emptied by the transport.
7-0	RL 7-0	@	Revision Level. On a Write Characteristics command this field displays the settings of the Extended Features Enable switch (bit 7) and the Buffering Enable switch (bit 6) and the microcode revision level (bits 5-0). On all other commands, bits 2-0 show the unit number of the currently selected transport.

3.3.2.8 Extended Status Register 3 (XST3) -- Extended Status Register 3 (XST3) appears as the seventh word in the Message Buffer stored by the TSV05 upon completion of a command or on an Attention (ATTN). Figure 3-12 illustrates the register format and Table 3-10 describes each bit.

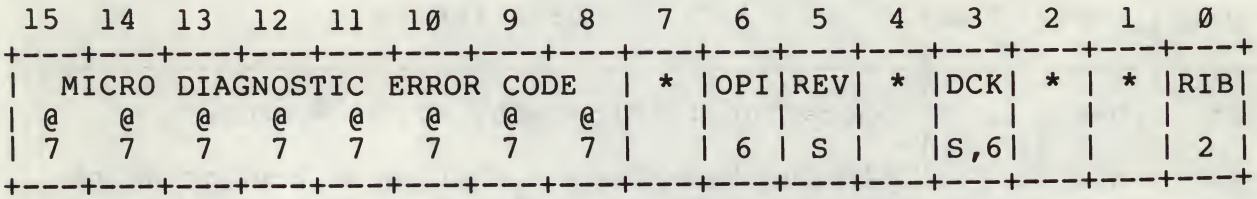


Figure 3-12 XST3 Register Format

Table 3-10 XST3 Register Bit Definitions

Bit	Name	Code	Description
15-8	MDE	7	Micro-Diagnostic Error Code. This field is encoded by the controller to indicate various failures detected by the microprogram. Detections can occur during the running of internal on-line tests during Idle periods (e.g., RAM or FIFO failures). Once an error occurs, an Initialize must be issued to use the controller again.
07	-	*	Not used by the TSV05. In the TS11, this bit is LMX - Tension Arm Limit Exceeded.
06	OPI	6	Operation Incomplete. Set when Read, Space, or Skip operation has moved about 25 feet of tape without detecting any data on the tape.
05	REV	S	Reverse. Set when the current operation caused reverse tape motion (includes the Retry commands as well as simply reverse Read, space, etc); clear when operation is forward or rewind.
04	-	*	Not used by the TSV0S, in the TS11, this BIT is CRF (Capstan Response Failure).

Table 3-10 XST3 Register Bit Definitions (Cont)

Bit	Name	Code	Description
Ø3	DCK	S,6	Density Check. Set when a PE Identification Burst (IDB) is not detected while moving off of BOT. A Read, Space or Skip will, however, complete (if no other errors occur) to allow tapes with the IDB wrong to be read.
2,1	-	*	Not used by the TSVØ5; always set to Ø. Bit 2 is used by the TS11 to indicate that a noise bit was detected during an erase. Bit 1 is used by the TS11 to indicate that a limit switch was activated.
ØØ	RIB	2	Reverse Into BOT. When set, indicates that a Read, Space, Skip or Retry command already in progress has encountered the BOT marker when moving tape in the reverse direction. Tape motion will be halted at BOT.

3.3.2.9 **Extended Status Register 4 (XST4)** -- Extended Status Register 4 (XST4) appears as the eighth word in the Message Buffer stored by the TSVØ5 upon completion of a or on an Attention (ATTN). Figure 3-13 illustrates the register format and Table 3-11 describes each bit. Note that for this word to be stored, the Extended Features option must be enabled and the Message Buffer extent parameter specified in the Write Characteristics command must be increased by 2 over the normal TS11 specification.

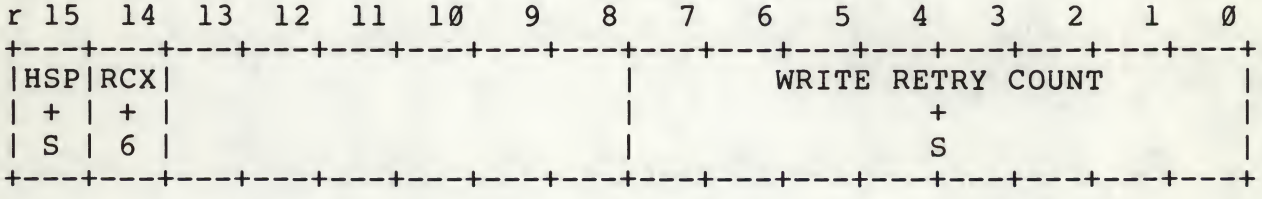


Figure 3-13 XST4 Register Format

Table 3-11 XST4 Register Bit Definitions

Bit	Name	Code	Description
15	HSP	S	High Speed. When set, indicates that the transport is operating in high speed mode (100 IPS). When clear, the transport is operating in low speed mode (25 IPS).
14	RCX	6	Retry Count Exceeded. When set, indicates that the controller was buffering Write data and could not successfully output the buffered record within the specified number of retries. Causes Tape Position Lost termination.
13-8	-	-	Reserved. Always set to 0.
7-0	WRC	S	Write Retry Count Statistic. When the controller is buffering write data records, this field indicates the total number of controller-initiated retries performed in order to write the previous buffered record. This count is cleared after it is displayed. For example, consider the situation in which 1) buffering is in operation and record N is in RAM (the controller has given successful termination for record N), and 2) the Write command for record N+1 has been issued to the controller but the controller has not yet accepted the command, and 3) the controller must perform M retries to finally write record N successfully. In this situation, M will appear in the WRC field when termination of record N+1 is finally given.

3.3.2.10 **Summary of Registers** -- The formats of the hardware and remote (software determined) registers discussed in the preceding sections are summarized in Figures 3-14 and 3-15. Figure 3-16 shows the format of the command registers implemented by the LSI-11 CPU when it builds a command packet.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSBA (R/O)	A15 S	A14 S	A13 S	A12 S	A11 S	A10 S	A09 S	A08 S	A07 S	A06 S	A05 S	A04 S	A03 S	A02 S	A01 S	A00 S
TSDB (W/O)	P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
TSSR (R/W)	SC S	*	SCE @ & S	RMR S	NXM 4,5	NBA S	A17 S	A16 S	SSR S	OFL S 1,3	FC1 7	FCO 7	TC2 S	TC1 S	TC0 S	
TSDBX (W/O)	BT				P21	P20	P19	P18								

(TSDBX exists only on the TSV05)

Legend:

* = Bit defined for TS11 but normally set to 0 by TSV05
@ = Bit defined for TS11 but has similiar but slightly different meaning for TSV05.
S = Status bit, not necessarily associated with a particular termination class.
1-7 = Termination class code associated with this bit.

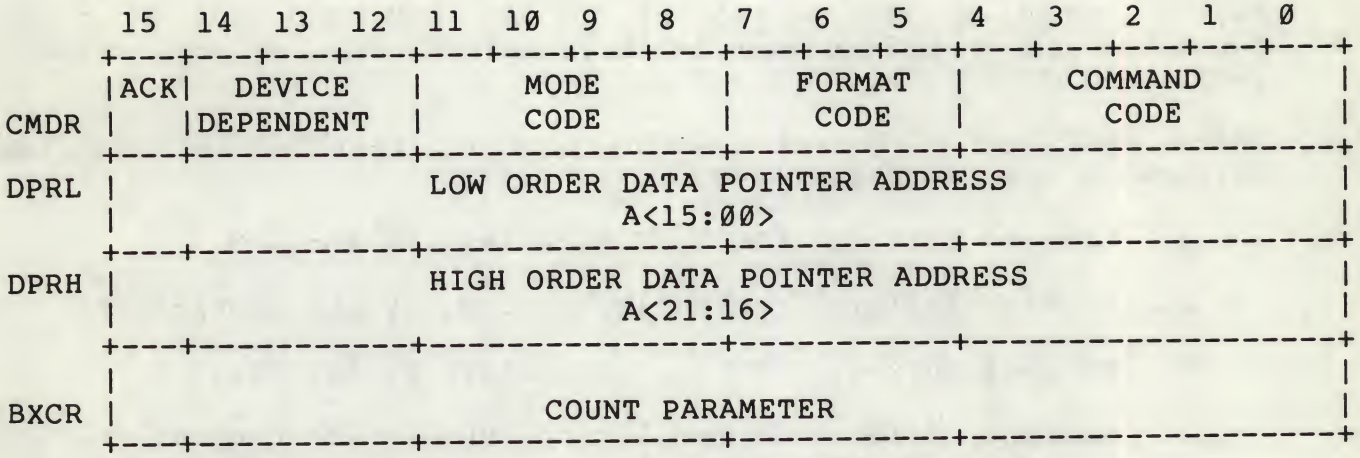
Figure 3-14 TSV05 Hardware Device Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XST0	TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT
										S						
	S,2	2	2	2	3.6	3	3	3	S	1,3	S	S,3	S	S,3	S,3	S,2
XST1	DLT		COR	*	*	*	*	RBP	*	*	*	*	*	*	UNC	*
								+								
	4		S,4					4							4	
XST2	OPM	RCE	*	*		WCF		*	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
		@							@	@	@	@	@	@	@	@
	S	7				7			S	S	S	S	S	S	S	S
XST3	MICRO DIAGNOSTIC ERROR CODE								*	OPI	REV	*	DCK	*	*	RIB
	@	@	@	@	@	@	@	@								
	7	7	7	7	7	7	7	7		6	S		S,6			2
XST4	HSP	RCX							WRITE RETRY COUNT							
	+	+							+							
	S	6							S							

Legend:

* = Bit defined for TS11 but normally set to 0 by TSV05.
@ = Bit defined for TS11 but has similiar but slightly different meaning for TSV05.
+ = Bit not defined (unused) in TS11.
S = Status bit, not necessarily associated with a particular termination class.
1-7 = Termination class code associated with this bit.
XST4 = Extended Status Register 4 not defined for TS11; Available in TSV05 when Message Buffer extent is increased.

Figure 3-15 TSV05 Extended Status Registers



NOTE: Not all words are required for all commands

Figure 3-16 TSV05 Command Register Format

3.3.3 Packet Processing

The CPU passes control information to the controller by means of a command packet in the Command Buffer area (e.g., a sequential series of control words) in CPU memory space. Similarly, the controller passes status information to the CPU by means of a message packet in the Message Buffer area in CPU Memory space. A command is initiated by the CPU by specifying to the controller the location of the Command Buffer (by writing TSDBX/TSDB). The controller then becomes "busy", fetches the command and associated parameters from the Command Buffer, executes the command, deposits status into the Message Buffer, and finishes by becoming idle. The CPU can then examine the TSSR hardware register and the Message Buffer to determine the success or failure of the command. Every command is handled in this basic manner. The following paragraphs discuss buffer control, Message Buffer format, and Attention handling.

The basic "packet protocol" scheme implemented by the TSV05 is identical to that implemented by the TS11/TS04 Magtape System. There are, however, differences in some of the information passed between controller and CPU. These differences are in the form of extra command modes and extra or differing status fields implemented by the TSV05 when the Extended Features switch is set. There is also a difference in operation of the Write Subsystem Memory diagnostic command, whether or not Extended Features are enabled. These differences are discussed within the descriptions of the individual commands. The basic protocol, however does not change.

3.3.3.1 Buffer Ownership and Control -- To prevent the controller from updating the Message Buffer while the CPU is reading it, or the CPU from updating the Command Buffer while the controller is reading it, the concept of "ownership" is defined. Each buffer may be owned by the controller or the CPU, but not by both. Ownership of a buffer can be transferred only by the current owner.

There are four different combinations of transferring the two buffers in the two directions:

1. Command Buffer: CPU to Controller, by the CPU.
2. Command Buffer: Controller to CPU, by the Controller.
3. Message Buffer: CPU to Controller, by the CPU.
4. Message Buffer: Controller to CPU, by the Controller.

Table 3-12 describes the buffer transfer operations.

An Initialize aborts any current operation and gives ownership of both the Command Buffer and the Message Buffer to the CPU.

Table 3-12 Buffer Ownership Transfers

Buffer	Direction	Transfer Method
Command Buffer	CPU to Controller	The CPU transfers ownership of the Command Buffer to the Controller by writing the address of the Command Buffer into the TSDB register. This clears the SSR bit in TSSR.
Command Buffer	Controller to CPU	The Controller transfers ownership of the Command Buffer back to the CPU by depositing a Message Packet (in the Message Buffer) that has the Acknowledge (ACK) bit set in the message header word. After the message is deposited by the controller, it sets the SSR bit in TSSR to indicate that the message is in the Message Buffer. If the message does not contain the ACK bit set, the CPU will know that the controller did not see the last Command Buffer and that the CPU still owns the Command Buffer. The command may be reissued by the CPU.

Table 3-12 Buffer Ownership Transfer

Buffer	Direction	Transfer Method
Message Buffer	CPU to Controller	The CPU transfers ownership of the Message Buffer to the controller by setting the ACK bit in the Command Buffer and then initiating the command by writing into TSDB. If the Command Buffer does not contain the ACK bit, the controller will know that the CPU did not see the last message buffer and the controller still owns it. The controller, in response to the CPU writing into TSDB, will set SSR and perform an interrupt (if the IE bit is set) without sending out a message, since it does not own the buffer.
Message Buffer	Controller to CPU	The Controller transfers ownership of the Message Buffer to the CPU by writing the Message Buffer and setting the SSR bit. This can happen at one of two times: 1. At the end of a command, or 2. By outputting an Attention (ATTN) message. In this case, SSR will already be 1 because an ATTN only happens when the controller is inactive. So the controller clears SSR, outputs the message, the sets SSR again (and interrupts if the IE bit was set on the Message Buffer Release Command that gave control of the Message Buffer to the Controller). Note that for an ATTN to occur, the EAI bit must have been set in the previous Write Characteristics command.

During normal command processing, the ownership of both buffers passes simultaneously, first from CPU to Controller (at the start of command processing, when the CPU writes a Command Pointer into the TSDB register), and then from Controller to CPU (upon completion of the command).

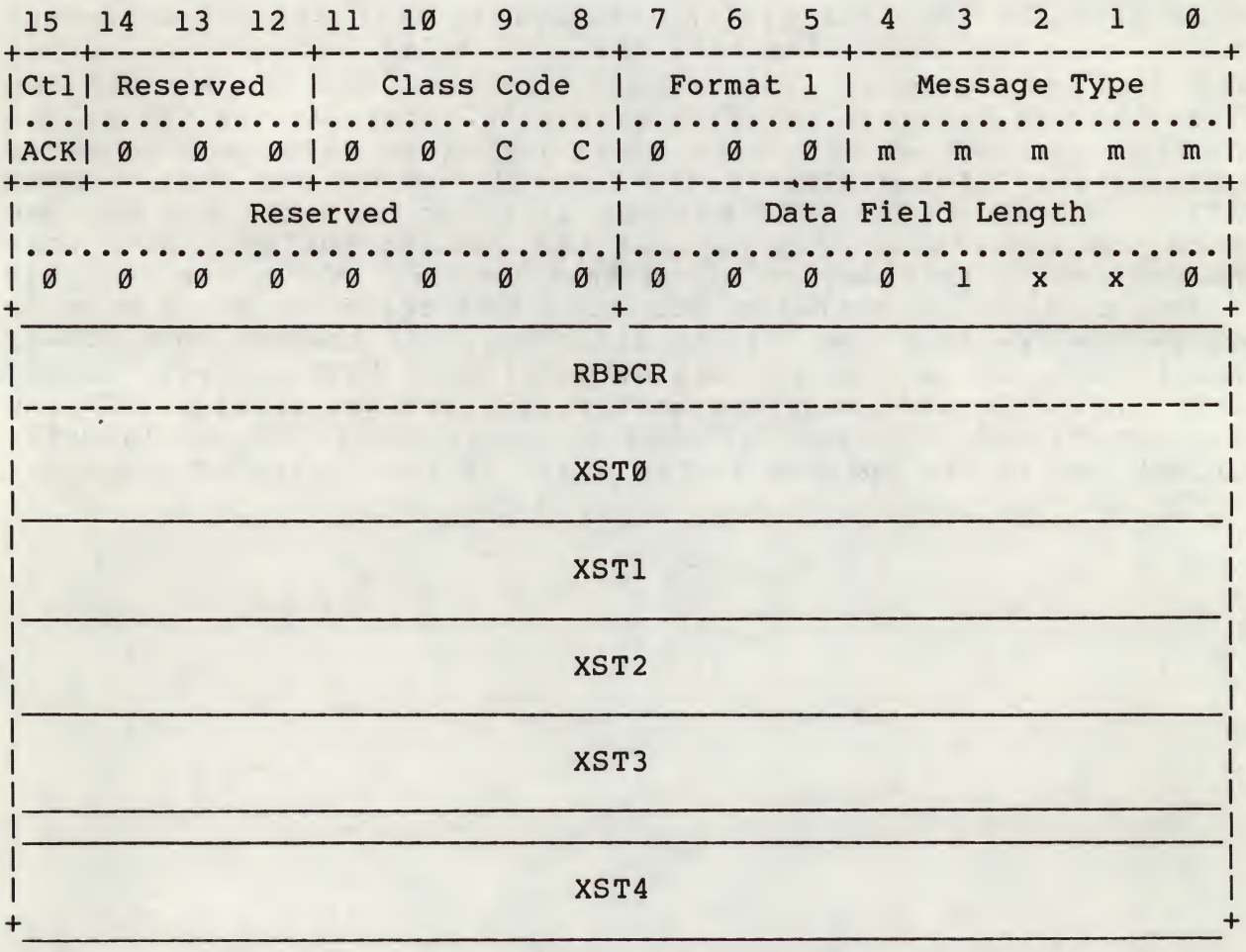
3.3.3.2 Buffer Control On Attentions -- An Attention (ATTN) is enabled by the CPU by setting up the appropriate Characteristics Mode word on the Write Characteristics command. It allows the controller to flag exceptional conditions (change in transport on-line/off-line status and microdiagnostic self-test errors) when the controller is in the Idle state (not executing a command). If an ATTN condition occurs and the controller does not own the Message Buffer, the controller will queue the ATTN internally. Then, when the CPU releases the Message Buffer on the next command (with the ACK bit set), the controller will output the ATTN message with the ACK bit Ø in the message header word to indicate that the command was lost (except for the transference of ownership of the Message Buffer to the controller). In this case, the controller refuses to accept ownership of the Command Buffer. The CPU will then still own the Command Buffer (because the controller did not accept the command) and will also own the Message Buffer now filled with an ATTN message. If the CPU still wants to do the ignored command, the CPU must reissue the command (with the ACK bit set). Exceptions to this procedure are the Write Characteristics command and Write Subsystem Memory command, which are executed regardless of a pending Attention. These exceptions are necessary to allow the software to specify a Message Buffer address, control enabling of Attentions, and perform diagnostics.

Now consider the case in which the CPU wants to be notified of a change in status or a microdiagnostic error while the controller is inactive for a long period of time. To accomplish this, the controller must own the Message Buffer for that entire period of time. Normally, the controller gives up ownership of the Message Buffer at the end of a command. However, for enabling Attention messages, ownership of the Message Buffer is transferred to the controller via the Message Buffer Release command. This is a special command that tells the controller not to give ownership of the Message Buffer back to the CPU at the end of the command. The controller does not output a message at the end of this command, but just updates the TSSR register (with the SSR bit set) and interrupts (if the IE bit was set in the command and such an interrupt was enabled by the ERI bit in the previous Write Characteristics command. The controller then maintains ownership of the Message Buffer until an ATTN condition is seen and then immediately clears SSR, outputs the ATTN message (with the ACK bit not set since the controller is not responding to a command), and then sets SSR and interrupts the CPU (if the IE bit was set on the Message Buffer Release command). In this condition, the CPU owns the Command Buffer and the Controller owns the Message Buffer. If the controller outputs an Attention message, ownership of the Message Buffer is passed to the CPU. At that time the system is back to the state of the CPU owning both buffers. Another ATTN will not be done until the CPU does a command with the ACK bit set to release ownership of the Message Buffer containing the ATTN message.

If the CPU has done a Message Buffer Release command, and wants to do another command but has not received an ATTN from the controller (so that the controller still owns the Message Buffer from the Message Buffer Release command), the CPU can do a command without the ACK bit set in the command buffer. At the time the command is issued, the CPU does not own the Message Buffer so the CPU cannot release the Message Buffer. If the CPU does set the ACK bit, nothing will happen except the CPU might miss an ATTN if the controller was sending out an ATTN message at the same time that the CPU was issuing the command.

It is possible that the CPU may attempt to initiate a new command at or near the same time that the controller attempts to output an Attention message. [The command must not have the ACK bit set since the CPU does not own the Message Buffer.] If the CPU writes the TSDB register while SSR is clear during an ATTN, the Register Modification Refused (RMR) error bit will be set and that command will be ignored. The ATTN message will not have the ACK bit set since the controller does not own the command buffer. Note that RMR may set in this way on a bug-free system. All other settings of RMR indicate a software bug (the CPU tried to do a command before the previous command was finished). If the CPU command was lost because the controller was outputting an ATTN message, Volume Check (VOL CHK) and Interrupt Enable (IE) are not updated. If the CPU command was rejected (illegal command, etc.) and not ignored, VOL CHK and IE are updated to the start of the rejected command.

3.3.3.3 Message Packet Format -- Figure 3-17 illustrates the format of the message packet in the Message Buffer. This format is used for all messages, whether at an end of a command or for an Attention. The message consists of a Header word, a Data Field Length word, a Residual Byte/Record/Tape-Mark Count word, and either four or five Extended Status registers. Normally, only four Extended Status registers are provided. The fifth one (XST4) is available only when the Extended Features function of the controller is enabled. Table 3-13 describes the message packet.



NOTE: XST4 is not part of a TS11-compatible Message Buffer. It is available only when the Extended Features mode is enabled.

Figure 3-17 Message Packet Format

Table 3-13 Message Packet Field Definitions

Word	Bit	Description
1 (Header)	15	ACK -- Acknowledge. This bit is set by the TSV05 to inform the CPU that the Command Buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit will not be set since the controller does not own the Command Buffer.
	14-12	Reserved. These bits are reserved for future expansion. They will always appear as zero.
	11-8	Class Code Field. These bits define the class of failure determined for the rest of the message buffer when the Message Type field is not indicating a normal END message. The codes are: Message Type / Class Code / Definition ATTN / 0000 / On or off line ATTN / 0001 / Microdiagnostic failure FAIL / 0000 / Not used. (On the TS11, this code indicates a Bad Packet due to a serial bus parity error.) FAIL / 0001 / Illegal Command (ILC), Illegal Address (ILA), or Need Buffer Address (NBA) on a tape motion command. FAIL / 0010 / Write-Lock error on Non-executable function. FAIL / 0011 / Microdiagnostic Error.
	7-5	Packet Format #1 Field. The single value supported by the TSV05 is 000, which specifies a one-word message header.

Table 3-13 Message Packet Field Definitions (Cont)

Word	Bit	Description
1	4-Ø	Message Type Code. This field, together with the Format field indicates the format and length of message packets. For the TSVØ5 (and TS11), the Message Type is of the form 1Øxxx, which indicates that the message contains a Header word, a Data-Cont'd| Length word and then xxx Data/Status words. This field indicates the general type of message contained in the buffer and is related to the Termination Class Code appearing in the TSSR register as follows: Termination Class Code / Message Type / Definition Ø,2 / 1ØØØØ / End 3 / 1ØØØ1 / Fail 4,5,6,7 / 1ØØ1Ø / Error 1,7 / 1ØØ11 / Attention
2 (Data Length)	15-8	Reserved. This field is reserved for future expansion. It always appears as Ø.
	7-Ø	Data Field Length. This field specifies how many bytes of information follow this word in the message packet. Normally, with the Extended Features option of the TSVØ5 disabled, this field contains a value of 1Ø (binary ØØØØ1Ø1Ø), indicating that the packet contains the RBPCR plus four Extended Status registers. With the Extended Features option enabled, this field contains a value of 12, to indicate that an additional Extended Status register (XST4) is supplied.

Table 3-13 Message Packet Field Definitions (Cont)

Word	Bit	Description
3 (RBPCR)	15-ØØ	Residual Byte/Record/File Count Register. After a Read command, this word contains the difference between the number of bytes specified in the command and the number of bytes actually transferred from tape. In other words, this register indicates by how much the tape record fell short of the expected length. After a Space Records or Skip Tape Marks command, this register contains the difference between the number of records or tape marks specified in the Count word of the command and the number of records or files actually skipped. Note that spacing and skipping operations can terminate before the count is exhausted for a variety of reasons (tape mark, BOT, etc.).
4 (XSTØ)	15-ØØ	Extended Status Register Ø. See Paragraph 3.4.2.5 for a description of this register.
5 (XST1)	15-ØØ	Extended Status Register 1. See Paragraph 3.4.2.6 for a description of this register.
6 (XST2)	15-ØØ	Extended Status Register 2. See Paragraph 3.4.2.7 for a description of this register.
7 (XST3)	15-ØØ	Extended Status Register 3. See Paragraph 3.4.2.8 for a description of this register.
8 (XST4)	15-ØØ	Extended Status Register 4. See Paragraph 3.4.2.9 for a description of this register. Note that this register is not supplied in TS11 Compatibility mode (Extended Features disabled).

3.3.3.4 General Status Handling Information -- Table 3-14 summarizes the relationship between the termination class code appearing in the TSSR register and Message Type code appearing in the Header Word of the Message Buffer after a message packet has been deposited by the controller.

Table 3-14 Termination Class/Message Type Relationship

TC2-Ø Value	Offset	Message Type	Meaning
Ø	ØØ	END (2Ø)	Normal Termination. The operation was completed without incident.
1	Ø2	ATTN (23)	Attention condition. This code indicates that the drive has undergone a status change, such as going Off-Line or coming On-Line.
2	Ø4	END (2Ø)	Tape Status Alert. A status condition has been encountered that may have significance to the program. Bits of interest in the Extended Status registers include TMK (Tape Mark), EOT (End of Tape) and RLL (Record Length Long).
3	Ø6	FAIL (21)	Function Reject. The specified function was not initiated. Bits of interest include OFL, VCK, BOT, WLE, ILC, and ILA.
4	1Ø	ERROR (22)	Recoverable Error. Tape position is a record beyond what its position was when the function was initiated. Suggested recovery procedure is to log the error and issue the appropriate retry command.
5	12	ERROR (22)	Recoverable Error. Tape position has not changed. Suggested recovery procedure is to log the error and reissue the original command.

Table 3-14 Termination Class/Message Type Relationship (Cont)

TC2-Ø Value	Offset	Message Type	Meaning
6	14	ERROR (22)	Unrecoverable Error. Tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers. Recovery would be handled by the specific application program.
7	16	ATTN (23) or ERROR (22)	Fatal Subsystem Error. The subsystem is incapable of properly performing commands, or at least its integrity is seriously questionable. Refer to the Fatal Class code field in the TSSR register for additional information on the type of fatal error.

The following points should be noted in reference to status and error handling:

1. Error bits in the TSSR register (SC and RMR) are cleared by successfully loading a command pointer into the TSDB register and by successfully depositing an END message.

2. All commands (even the Get Status command) clear the internal copy of each error bit in the Extended Status registers except bits 15-8 of XST3 (Microdiagnostic Error Code). Therefore, a Get Status command will not return the error bits as set up by a previous tape operation.

3. A Read operation which encounters a Tape Mark will not transfer any data and will give a Tape Status Alert termination. The Tape Mark and Record Length Short status bits will be set, and the RBPCR word in the message buffer will contain the original byte count as specified in the command.

4. A Space Records operation will automatically terminate when a Tape Mark is traversed, and the TMK status bit will be set. Also, Record Length Short (RLS) will be set if the record count was not decremented to zero.

5. A Skip Tape Marks operation will automatically terminate when two consecutive tape marks are encountered and the "Enable Skip Stop" (ESS) mode is enabled via the Write Characteristics command. Record Length Short (RLS) will be set if the count was not decremented to zero. The same is also true if a tape mark is the first record off BOT and both the ESS and ENB bits were set in the previous Write Characteristics data word.

6. Every Write, Write Retry, Write Tape Mark, Write Tape Mark Retry, and Erase command which is executed at or beyond the EOT marker will result in a Tape Status Alert termination. The internal EOT status bit will remain set until logically passed over in the reverse direction (Rewind, reverse Read, reverse Space, etc.). The EOT status bit is not specifically identified with a particular record.

7. A Read Reverse, Space Reverse, Reverse or Skip Tape Marks Reverse command which encounters BOT after the operation is underway will result in a Tape Status Alert termination (the RIB status bit will be set).

8. If a Read Reverse, Space Records Reverse, or Skip Tape Marks Reverse command is issued while the tape is already at BOT, a Function Reject (NEF-Non-Executable Function) status will be returned.

9. When a normal Rewind command is issued, the termination message and interrupt will not occur until the tape reaches BOT and has stopped. If the tape space is already at BOT when the command is issued, the transport will still be commanded to rewind to make sure the tape is properly positioned.

10. When a Rewind with Immediate Interrupt is issued, the controller commands the transport to rewind, checks for proper status, and then issues an interrupt and END message for normal termination. If a new tape motion command is issued to a rewinding unit, the controller will wait until the tape has been rewound to BOT before preceding with the new command. During execution of a Rewind with Immediate Interrupt, the Motion (MOT) bit in XSTO will be set if a Get Status command is performed.

11. Any Write Function issued at BOT (including Erase which results in the Density Check bit (DCK) being set will cause a termination of that command with a TSSR Termination Class code of 6 set to indicate an unrecoverable error. Normally, a Write function causes the PE Identification (ID) burst to be written off BOT, and the controller checks for the appropriate status signal from the transport. Therefore, if DCK is set on a write off BOT, a serious transport or controller problem exists.

12. If a Density Check condition is detected during a Read, Space or Skip Function, the DCK bit will be set but the operation will not be aborted. If DCK is the only error status bit set during the operation, normal termination will be reported. This allows tapes with good data but bad denisty check (ID) areas to be read. If, in fact, a tape of the wrong density has been mounted, other errors will be reported and will stop the operation.

13. Note that if you begin reading a tape, get a Density Check with no other errors, and then append data to the tape, the Write will get a Termination Class code of 6 indicating that tape position is lost because Density Check will remain set. The whole tape should be copied over so that drives that depend on the ID burst will be able to read the tape.

14. Certain failures can result in no interrupt even though the specified command had Interrupt Enable set. These failures include NXM (Non-Existent Memory Error), since the failure could have occurred before the Interrupt Enable bit was fetched from the command packet.

15. The following are notes concerning interrupts:

a. If interrupts are enabled (the Interrupt Enable bit was set on the previous command accepted by the controller), interrupts may occur at any time. This is due to the possiblity of diagnostic interupts occurring immediately after normal terminations (even if Attention interrupts are not enabled). The software must therefore defend against unexpected interrupts. The subsystem may not be useable, but the software should still not crash.

b. Similarly, the controller could be broken in such a way that interrupts may be issued even with IE clear.

c. With Attention interrupts enabled (EAI bit set on the Write Characteristics command), a non-fatal diagnostic failure will not be reported until control of the Message Buffer is returned to the controller. A fatal failure may interrupt at any time as lone as Interrupt Enable is set.

d. With Attention interrupts disable, a diagnostic failure will not be noticable until the next command is issued. At this time, the command will be rejected.

e. When record buffering for Writes is in operation, the controller issues Normal Termination messages and interrupts immediately after the data to be written has been stored in the controller's RAM and before the data is actually written on tape. The possiblity exists that the record cannot successfully be written on tape with the first attempt, in which case a retry algorithm is executed to attempt to successfully write the data. If the data is eventually successfuly written, the CPU will not know that any problem occurred unless the Extended Features option is enabled, in which case the Write Retry Count field in XST4 can be examined in the message termination the NEXT command. If retries are therefore to be logged, the software should examine the Write Retry Count field in each message packet.

f. If record buffering for Writes is in operation and the controller cannot write a stored record successfully from its RAM (retry count exhausted), the next Tape Motion command following the Write command associated with the failed record will be terminated with Termination Class 6 (Tape Position Lost) and the Retry Count Exceeded (RCX) bit in XST4 will be set. In addition, the Uncorrectable Error (UNC) bit in XST1 will be set. The tape will be positioned one record beyond the last successfully written record.

3.3.4 Commands

The TSVØ5 is capable of running on programs that are, in most cases, identical to those written for the TS11/TsØ4 Magtape Subsystem. When the Extended Features option of the TSVØ5 is disabled, the following commands and their associated command modes operate identically to those of the TS11, except for some of the extended error status bits provided for by the TS11 but not by the TSVØ5.

READ
WRITE
POSITION
FORMAT
GET STATUS

With Extended Features enabled, the above commands have the capability to perform 22-bit memory addressing, and, in addition, some command modes (subcommands) are added that are not in the TS11 repertoire: basic operation of the basic TS11 commands, however, remains the same.

The following commands differ in their meanings to TSVØ5 and TS11 hardware:

WRITE CHARACTERISTICS (Same as TS11 except for the ability, when the Extended Features switch is set, of the TSVØ5 to specify an extra Characteristics Data word to control special features, and also to specify a longer than normal Message Buffer length to accommodate an extra Extended Status register).

WRITE SUBSYSTEM MEMORY (The data format and function is entirely different from that of the TS11).

CONTROL (Function is same as TS11 except for the Clean Tape command mode, which the TSVØ5 treats as a NO-OP -- tape is not moved. In addition, when Extended Features is enabled, two new command modes are added).

INITIALIZE (Similar to TS11 in that control logic is initialized but the transport itself is not initialized in certain non-error states.)

The following paragrpahs first describe the general command format, then each command is described in detail.

3.3.4.1 Command Packet Definitions -- The CPU issues a command to the TSVØ5 subsystem by first building a Command Packet in CPU memory space (on a modulo-4 address boundary) then writing the address of the packet into the TSVØ5 TSDB hardware register. The address written is termed the Command Pointer. Assuming that the TSVØ5 is ready to accept a command, writing of the Command Pointer initiates command processing, in which the controller fetches the Command Packet and executes the command encoded within the packet.

Logically, a Command Packet can be composed of one, two, three or four 16-bit words, depending upon the type of command and the amount of information it needs to proceed with execution. All Command Packets begin with a Command Packet Header Word, shown in Figure 3-18. The format of this word is the same for all commands; the encoding of the various fields within the word distinguishes one command from another. Table 3-15 defines the fields within the Header Word. Table 3-16 summarizes the Command Code and Command Mode field definitions. The following paragraphs describe each command in detail, along with its specific Command Packet format. Figure 3-18 illustrates the positioning of tape data bytes in CPU memory under various conditions (Forward, Reverse, Swap Bytes, etc.) for Read and Write commands.

Certain bits of the Header Word and other words within the Command Packet are not defined for all commands. When building the Command Packet, the software should set these undefined bits to zero. If any bit is undefined or reserved with respect to a particular command and the bit is not zero, the command will not be executed and will be terminated with a Function Reject (Termination Class 3).

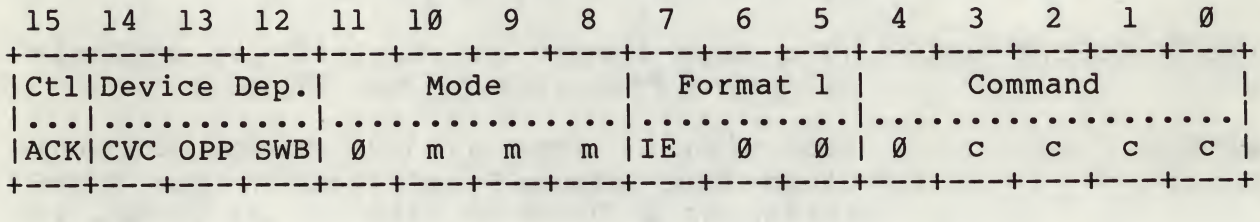


Figure 3-18 Command Packet Header Word

Table 3-15 Command Packet Header Word Bit Definitions

Bit	Name	Function
15	Acknowledge (ACK)	This bit should be set when issuing a command when the CPU owns the Message Buffer. Its function is to inform the TSVØ5 that the Message Buffer is now available for any pending or subsequent message packets. This passes ownership of the Message Buffer to the TSVØ5 controller. If the CPU has released ownership of the Message Buffer to the TSVØ5 for Attentions and has not received an ATTN message yet, the ACK bit should be coded as a Ø.
14-12	Device Dependent Bits	These three bits perform functions applicable to particular commands. The bit definitions are as follows: Bit — Name — Definition 14 — CVC — Clear Volume Check - When set, causes the Volume Check condition, set when the transport goes from Off-Line to On-Line, to be cleared, thereby allowing tape operations to be executed on the transport. 13 — OPP — Opposite - When set, reverses the execution sequence of reread commands (i.e, Reread Next, Previous, etc) 12 — SWB — Swap Bytes - When set, instructs the TSVØ5 to alter the sequence of storing and retrieving tape data bytes from the CPU memory. When SWB=Ø, the "first" byte in a word is the least significant byte (bits 7-Ø); this is the standard DEC method. When SWB=1, an industry-standard method is specified, in which the first byte of a word is considered to be bits 15 through 8. Figure 3-19 illustrates the positions of bytes as written or read from memory.

Table 3-15 Command Packet Header Word Bit Definitions (Cont)

Bit	Name	Function
11-8	Command Mode Field	This field acts as an extension to the Command Code field and allows further specification of device commands, as detailed in Table 3-16.
7-5	Packet Format #1 Field	This field defines the header type (only one type is used in the TSV05 and TS11) and the Interrupt Enable. The only two valid configurations are: Bit Values — Definition 000 — One-word Header; Interrupt Disable 100 — One-word Header; Interrupt Enable
4-0	Command Code	This field defines that major command category. It is used together with the Command Mode field to specify the command, as defined in Table 3-16.

Table 3-16 Command Code and Mode Field Definitions

Command Code	Command Name	Command Mode	Mode Name
00001	READ	0000	- Read Next (Forward)
		0001	- Read Previous (Reverse)
		0010	- Reread Previous (Space Reverse, Read Forward)
		0011	- Reread Next (Space Forward, Read Reverse)
00100	WRITE CHARACTERISTICS	0000	- Load Message Buffer address and Set Device Characteristics
00101	WRITE	0000	- Write Data (Next)
		0010	- Write Data Retry (Space Reverse, Erase, Write Data)
00110	WRITE SUBSYSTEM MEMORY	0000	- Enter Maintenance Mode and Load Test Functions (diagnostic use only)
01000	POSITION	0000	- Space Records Forward
		0001	- Space Records Reverse
		0010	- Skip Tape Marks Forward
		0011	- Skip Tape Marks Reverse
		0100	- Rewind
01001	FORMAT	0000	- Write Tape Mark
		0001	- Erase
		0010	- Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)
01010	CONTROL	0000	- Message Buffer Release
		0001	- Rewind and Unload
		0010	- NO-OP (Performs Clean Tape function in TS11)
		0100*	- Rewind with Immediate Interrupt
01011	INITIALIZE	0000	- Controller/Drive Initialize
01111	GET STATUS	0000	- Get Status (output END status message)

* Extended Features function, not part of the TS11 repertoire.

Swap Bytes = Ø
Buffer Address = 1ØØØ
Byte Count = 1Ø(8)
Block Size = 1Ø(8) bytes

1ØØØ	1	Ø
1ØØ2	3	2
1ØØ4	5	4
1ØØ6	7	6

Swap Bytes = 1
Buffer Address = 1ØØØ
Byte Count = 1Ø(8)
Block Size = 1Ø(8) bytes

1ØØØ	Ø	1
1ØØ2	2	3
1ØØ4	4	5
1ØØ6	6	7

Swap Bytes = Ø
Buffer Address = 1ØØ1
Byte Count = 1Ø(8)
Block Size = 1Ø(8) bytes

1ØØØ	Ø	
1ØØ2	2	1
1ØØ4	4	3
1ØØ6	6	5
1Ø1Ø		7

Swap Bytes = 1
Buffer Address = 1ØØ1
Byte Count = 1Ø(8)
Block Size = 1Ø(8) bytes

1ØØØ		Ø
1ØØ2	1	2
1ØØ4	3	4
1ØØ6	5	6
1Ø1Ø	7	

NOTE
Byte Ø indicates the byte nearest to BOT.

Figure 3-19 (a) Memory/Tape Data Byte Positioning (Forward Tape Direction, Read or Write; Reverse Read with Even Byte Count)

Swap Bytes = Ø
Buffer Address = 1ØØØ
Byte Count = 7
Block Size = 7 bytes

1ØØØ	1	Ø
1ØØ2	3	2
1ØØ4	5	4
1ØØ6		6

Swap Bytes = 1
Buffer Address = 1ØØØ
Byte Count = 7
Block Size = 7 bytes

1ØØØ	Ø	1
1ØØ2	2	3
1ØØ4	4	5
1ØØ6	6	

Swap Bytes = Ø
Buffer Address = 1ØØ1
Byte Count = 7
Block Size = 7 bytes

1ØØØ	Ø	
1ØØ2	2	1
1ØØ4	4	3
1ØØ6	6	5

Swap Bytes = 1
Buffer Address = 1ØØ1
Byte Count = 7
Block Size = 7 bytes

1ØØØ		Ø
1ØØ2	1	2
1ØØ4	3	4
1ØØ6	5	6

NOTE
Byte Ø indicates the byte nearest to BOT.

Figure 3-19 (b) Memory/Tape Data Byte Positioning
(Forward or Reverse Read, Odd Byte Count)

3.3.4.2 Get Status Command -- Figure 3-20 illustrates the Get Status command packet. This command causes a message packet to be deposited in the Message Buffer area in order to update the Extended Status registers. However, after the end of any command except Message Buffer Release, the TSV05 hardware automatically updates the Extended Status registers, so this command need be used only when the TSV05 has been left idle for some time, or when a status register update is desired without performing a tape motion command, or when the user desires to read the unit number of the currently selected tape transport (deposited in bits 2-0 of Extended Status Register 2).

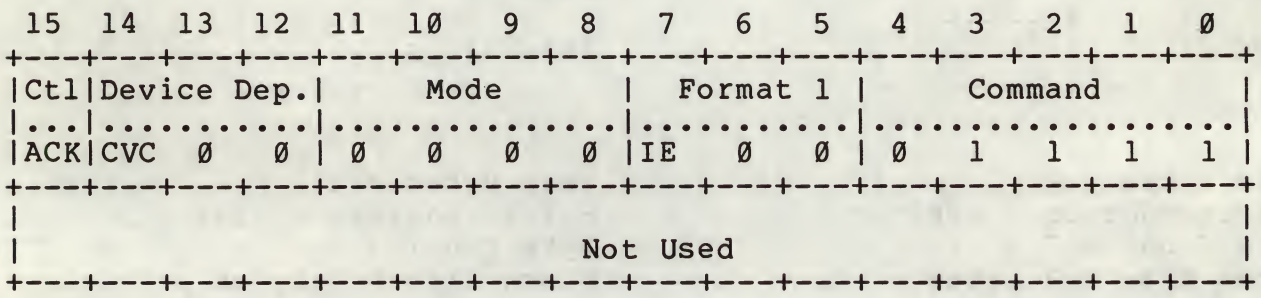


Figure 3-20 Get Status Command Packet

3.3.4.3 Read Command -- Figure 3-21 illustrates the command packet for a Read. There are four normal modes of operation: Read Forward, Read Reverse, Reread Previous, and Reread Next. Two of these modes (the Rereads) are further controlled by the state of the Opposite (OPP) bit in the packet header word.

Mode	Function
0000	Read Next (Forward)
0001	Read Previous (Reverse)
0010	Reread Previous
OPP = 0:	Space Reverse, Read Forward
OPP = 1:	Read Reverse, Space Forward
0011	Reread Next
OPP = 0:	Space Forward, Read Reverse
OPP = 1:	Read Forward, Space Reverse

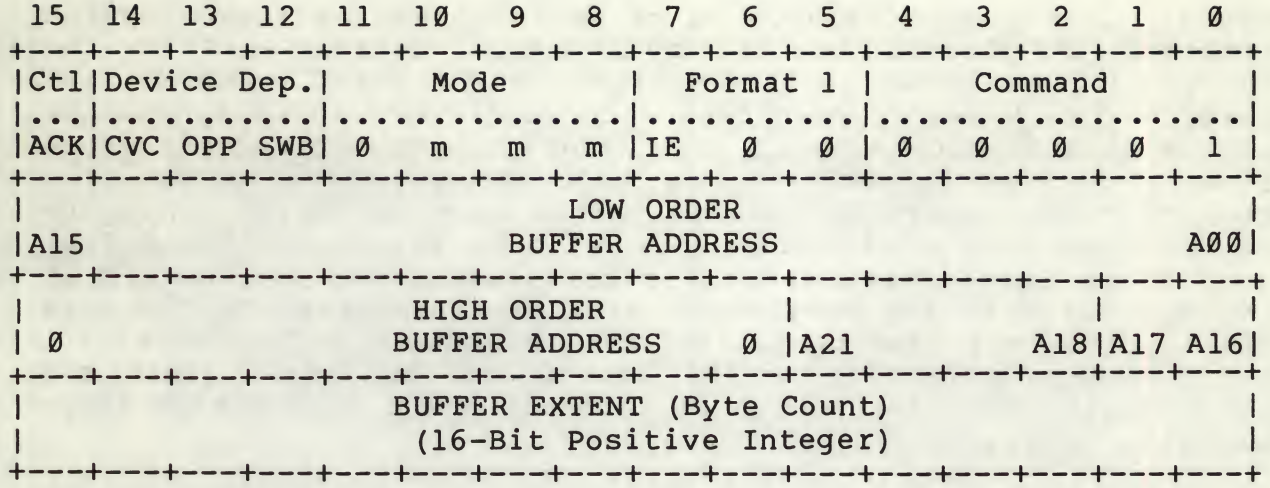


Figure 3-21 Read Command Packet

The command packet for a Read contains four words: a Header word, two words specifying the address of the data buffer in CPU memory space where the data read from tape is to be deposited, and a Buffer Extent (Byte Count) word specifying the number of bytes available in the data buffer and the number of bytes expected in the tape record to be read. A byte count of 0 specifies that 65,536 (64K) bytes are expected.

The third word in the packet specifies the high-order address bits of the starting address of the data buffer. When the Extended Features option is disabled (i.e., the TSV05 is running in TS11 compatibility mode), only the two low-order bits (A17 and A16) may be nonzero; these bits, together with the 16 bits in the second word of the packet allow an 18-bit memory address to be specified for the start of the data buffer. In this case, if any of bits 2-15 are nonzero, the function will not be performed but will terminate with a Function Reject with Illegal Address (ILA) error status. When the Extended Features mode is enabled, the low-order 6 bits of the third word are used to specify bits A21-A16 of a 22-bit memory address. In this mode, if any of bits 6-15 in the third word are nonzero, the command is aborted with Function Reject termination with Illegal Address (ILA) error status.

The read operation is assumed to be for a record of known length. Therefore, the correct record byte count (fourth word of the packet) must be known. If the byte count exactly equals the record length, Normal termination occurs. If the record is shorter than the specified byte count, the Record Length Short (RLS) error bit will be set in XSTØ and a Tape Status Alert termination occurs. If the record on tape is larger than the byte count, the Record Length Long (RLL) error bit will be set in XSTØ and Tape Status Alert termination given; in this case, only the number of bytes specified in the byte count will be transferred to the data buffer. Also, any Read operation that encounters a Tape Mark will not transfer any data. In this case, the Tape Mark (TMK) and Record Length Short (RLS) bits will be set and a Tape Status Alert termination given.

Reverse Read operations which pass BOT cause the Reverse Into BOT (RIB) bit in XST3 to be set and Tape Status Alert termination given. If the tape is already at BOT when a reverse read (i.e., Read Previous or Reread Previous with the OPP bit set) is issued, there will be no tape motion and Function Reject termination will occur, with the Non-Executable Function (NEF) error bit set in XSTØ.

The OPP bit in the header word (bit 13) alters the execution sequence of the Reread command modes, as follows:

1. Reread Previous (Space Reverse, Read Forward) becomes Read Reverse, Space Forward.

2. Reread Next (Space Forward, Read Reverse) becomes Read Forward, Space Reverse.

Reading data in the reverse direction with a correct byte count will place data in memory correctly (as if the record were read in the forward direction), not in reverse order. This feature allows data to be placed correctly in memory on one retry (read reverse). On a reverse read, data is placed in the data buffer in the reverse order (highest address first); the starting address is calculated by adding the byte count to the address specified in the command packet and then subtracting 1. if the byte count is greater than the actual record length, the beginning of the data buffer (lowest addresses) will not contain the data from tape. Similarly, if the actual record is larger than the byte count, the first part of the record (that nearest to BOT) will not be placed in the data buffer.

For any of the data transfers, the Swap Bytes (SWB) bit in the command header word controls the storing of bytes in CPU memory, as shown in Figure 3-19.

3.3.4.4 **Write Characteristics Command** -- Figure 3-22 illustrates the Write Characteristics command packet and data format. The objective of this packet is to inform the TSVØ5 subsystem of the location and size of the Message Buffer in the CPU memory space. The Message Buffer must be at least seven contiguous words long (eight when the Extended Features option is enabled) and located on a word boundary.

The Write Characteristics command also transfers a Characteristics Mode word to the controller and, if Extended Features is enabled, an additional control word. The Characteristics Mode word causes specific actions for certain operational modes. The bits for this word are defined in Table 3-17. Table 3-18 defines the bits in the additional control word available when Extended Features is enabled.

The four command packet words are identical to those used for the TS11 except for the third word (High Order Characteristic Data Address). In this word, bits 2 through 5 are used to specify bits 18 through 21, respectively, of the address specifying the location of the associated Characteristics Data buffer. The data buffer must reside on an even address in CPU memory space. If bit Ø of the second packet word (Low Order Characteristic Data Address) or bits 2-15 (Extended Features disabled) or bits 6-15 (Extended Features enabled) of the third packet word (High Order Characteristic Data Address) are nonzero, the function is not executed but is terminated with a Function Reject. In this case, no message packet is stored but an interrupt is generated if the IE bit is set. When the Extended Features switch on the M7196 module is off, the Write Characteristics command functions identically to that of the TS11. When the Extended Features switch is on, a fifth Characteristics Data word can be specified to invoke special functions. In addition, a Message Buffer Extent of 16 bytes (8 words) can be specified so that Extended Status Register 4 (unique to the TSVØ5) can be outputed.

Similarly, the first four words of the five-word Characteristic Data buffer are identical to those used for the TS11 except for the third word (High Order Message Buffer Address). In this word, bits 2 through 5 are used to specify bits 18 through 21, respectively, of the address specifying the location of the Message Buffer to be used for subsequent status and attention messages.

The fifth Characteristic Data word is used to specify parameters for the multi-record buffering mode of operation and also is used to select a tape unit in a multi-drive system. Table 3-18

The Write Characteristics command will clear the Need Buffer Address (NBA) bit in the TSSR register, indicating that a valid Message Buffer has been specified, if all of the following conditions are met:

1. The command was not rejected because of nonzero bits in reserved or unused fields within the first three command packet words,

2. The fourth packet word (Byte Count) contains at least a count of 6, to allow first three Characteristic Data words to be fetched,

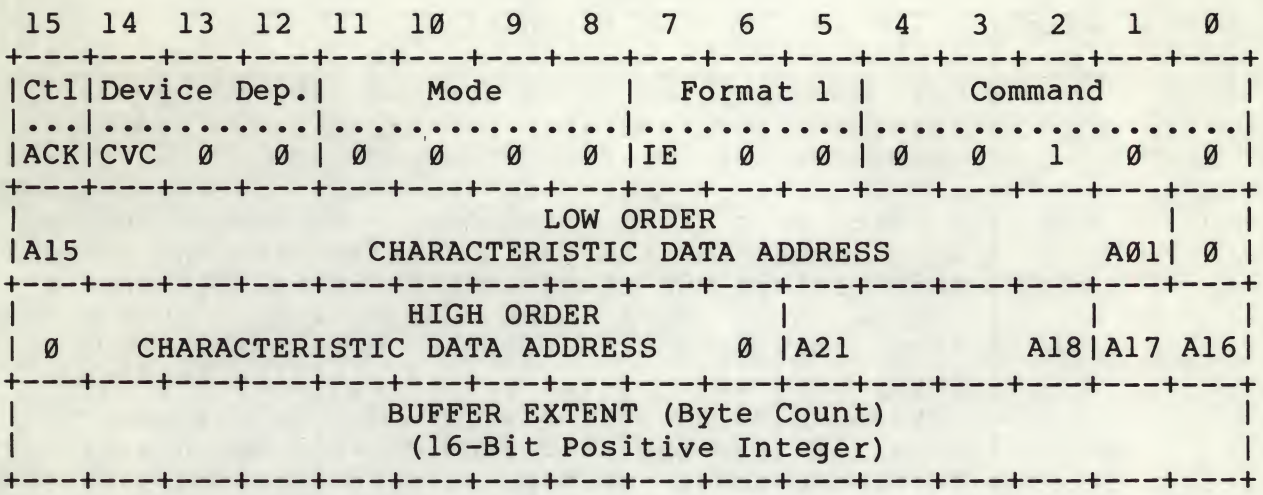
3. The first two Data words specify a valid even address (word boundary), and

4. The third Data word contains a value of 14 or greater (specifying the length of the Message Buffer).

If any of the above conditions are not met, then the NBA bit will be set (even if it was already clear from a previous valid Write Characteristics command) and no further message packets will be deposited.

Note that if the Byte Count word in the command packet is less than 7, the Characteristic Mode data word will not be fetched, causing the current values of the Characteristic Mode bits stored in the controller to be retained. Similarly, if the Byte Count is less than 10, the additional Extended Features control word will not be fetched and the current values retained.

(Command Packet)



(Characteristics Data)

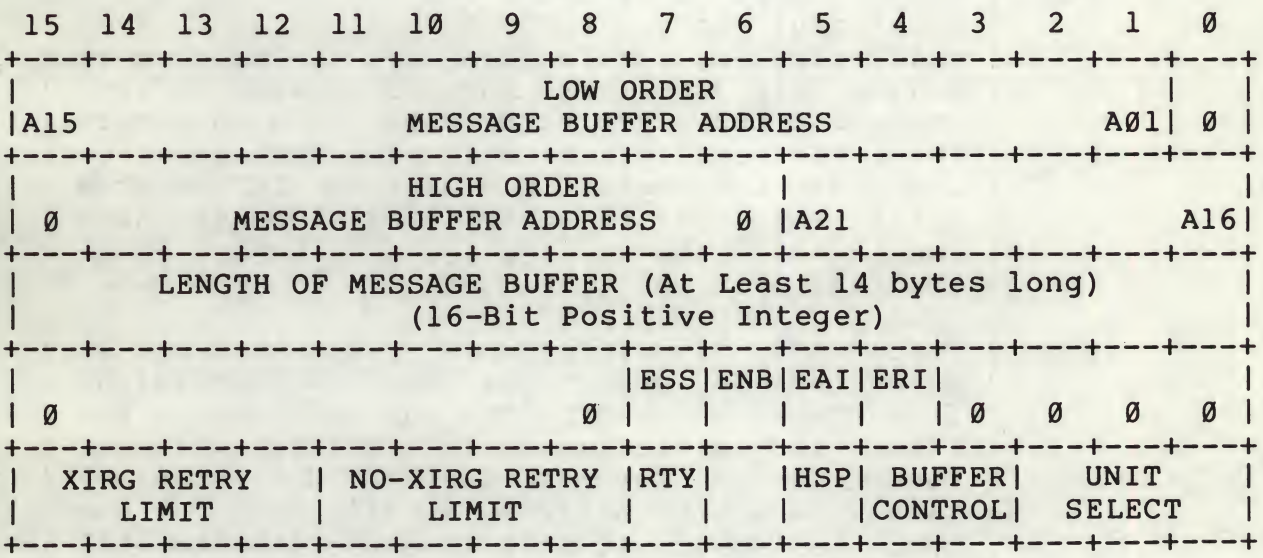


Figure 3-22 Write Characteristics Command Format

Table 3-17 Characteristic Mode Data Word Bit Definitions

Bit	Name	Definition
15-Ø8 3-Ø	-	Not used. These bits are not checked by the TSVØ5 controller. Their state will not affect operation but they should be written to Ø.
7	ESS	Enable Skip Tape Marks Stop - When set, this bit instructs the controller to stop and set the Logical End of Tape (LET) status bit during a Skip Tape Mark command when a double tape mark (two contiguous tape marks) have been detected. Setting this bit also enables operation of the ENB bit. In the default setting of Ø, the Skip Tape Marks command will terminate only on tape mark count exhausted, if it runs into BOT, or if it runs 15 feet past the EOT marker.
6	ENB	Enable Tape Mark Stop Off BOT - This bit is meaningful only if the ESS bit is set. When this bit is set (and ESS=1), the tape is at BOT, a Skip Tape Marks Forward command is issued, and the first record seen is a tape mark, then the controller will stop the operation and set the Logical End of Tape (LET) status bit in XSTØ. If this bit is clear under these conditions, the controller will merely count the tape mark and continue.
5	EAI	Enable Attention Interrupts - When this bit is Ø, attention conditions such as transitions from On-Line to Off-Line and Off-Line to On-Line, and microdiagnostic failures will not result in interrupts to the CPU. Rather, a tion will not be noticeable until the next command is issued; at this time the command will be rejected. With this bit set to 1, attention conditions will cause an Attention message to be generated (and an interrupt, if the IE bit was set on the last command) as soon as the controller owns the Message Buffer.
4	ERI	Enable Message Buffer Release Interrupts - If this bit is Ø, interrupts will not be generated upon completion of a Message Buffer Release command. Upon recognition of the command, only Subsystem Ready (SSR) will be reasserted. If ERI is 1, and interrupt will be generated (without an accompanying message packet).

Table 3-18 Extended Characteristics
Data Word Bit Definitions

Bit	Name	Description
15-12	XGRL	Extended Interrecord Gap (XIRG) Retry Limit. The value in this field, taken as a 4-bit positive integer, specifies the number of times the controller will attempt to write a buffered record before aborting buffered Write operation. A retry with XIRG consists of a backspace over the faulty record, an erase of 3.5 inches of tape, then a write of the buffered record (from RAM). An XIRG retry is attempted once after the Non-XIRG retry limit has been reached; then, if still not successful another series of non-XIRG retries is attempted. The total number of retries allowed on any record is therefore the Non-XIRG Limit times the XIRG Limit. This field has meaning only if write buffering is enabled and bit 7, RTY, is set.
11-8	NXGRL	Non-Extended Interrecord Gap Retry Limit. The value in this field, taken as a 4-bit positive integer, specifies the number of times the controller will attempt to write a buffered record without generating an extended IRG before attempting a retry with an extended IRG. A retry without an XIRG consists of a backspace over the faulty record, then a write of the buffered record (from RAM); no special erase is performed. This field has meaning only if write buffering is enabled and bit 7, RTY, is set.

Table 3-18 Extended Characteristics
Data Word Bit Definitions (Cont)

Bit	Name	Description
7	RTY	Retry Algorithm Control. When this bit is Ø and the controller is Write buffering, the default Retry algorithm (1 backspace then write with extended IRG, up to 1Ø times) is used when a record cannot be successfully written onto tape. When this bit is 1, the retry limits in bits 8-15 are used.
5	HSP	High-Speed Select. When this bit is Ø, the transport operates at a tape speed of 25 inches per second. When 1, the transport operates at 1ØØ inches per second.
4,3	BUF CTL	Buffering Mode Control. This 2-bit field controls the read and write buffering capabilities of the controller. The codes are defined as follows: Bit 4 / Bit 3 / Function Ø / Ø / Buffering is enabled or disable via the switch setting on the module. This is the default condition. Ø / 1 / No buffering is performed; the switch is ignored. 1 / Ø / Enable Read buffering only; the switch is ignored. 1 / 1 / Enable both Read and Write buffering; the switch is ignored.
2-Ø	USEL	Unit Select. This field selects a transport for subsequent tape operations. Initialize always sets the unit selection to Ø.

3.3.4.5 Write Command -- Figure 3-23 illustrates the command packet for a Write. There are two normal modes of operation: Write Data and Write Data Retry.

The allowable Mode field codes and their functions are:

Mode	Function
ØØØØ	Write Data
ØØ1Ø	Write Data Retry (Space Reverse, Erase, Write Data)

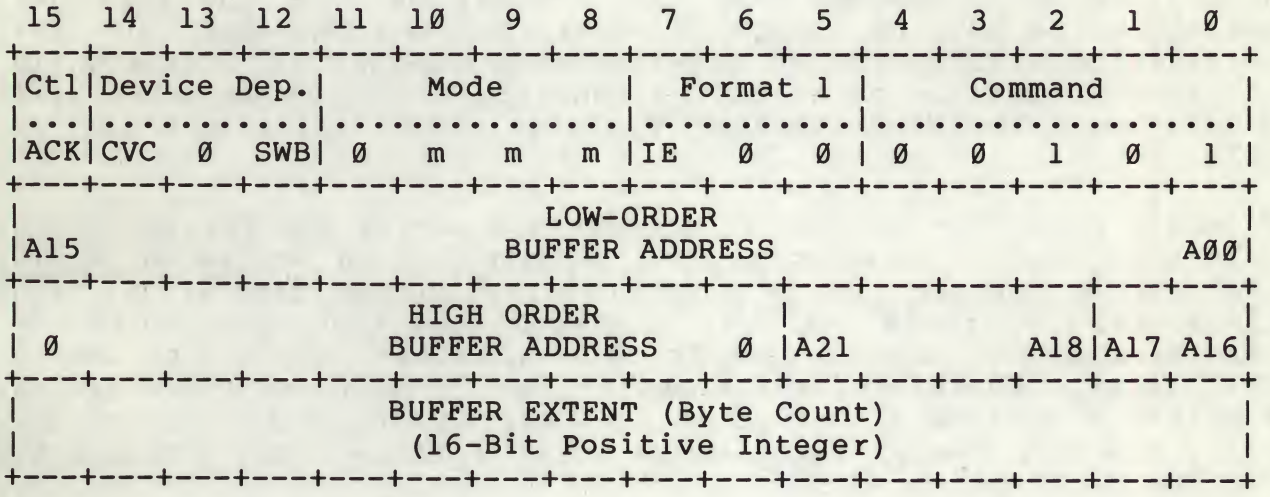


Figure 3-23 Write Command Packet

The command packet for a Write contains four words: a header word, two words specifying the address of the data buffer in CPU memory space where the data to be written onto tape is stored, and a Buffer Extent (Byte Count) word specifying the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of Ø specifies that 65,536 (64K) bytes are to be written.

The third word in the packet specifies the high-order address bits of the starting address of the data buffer. When the Extended Features option is disabled (i.e., the TSVØ5 is running in TS11 compatibility mode), only the two low-order bits (A17 and A16) may be nonzero; these bits, together with the 16 bits in the second word of the packet allow an 18-bit memory address to be specified for the start of the data buffer. In this case, if any of bits 2-15 are nonzero, the function will not be performed but will terminate with a Function Reject with Illegal Address (ILA) error status. When the Extended Features mode is enabled, the low-order 6 bits of the third word are used to specify bits A21-A16 of a 22-bit memory address. In this mode, if any of bits 6-15 in the third word are nonzero, the command is aborted with Function Reject termination with Illegal Address (ILA) error status.

For any of the Write modes, the Swap Bytes (SWB) bit in the command header word controls the fetching of bytes from CPU memory, as shown in Figure 3-19.

If a Write command is executed at or beyond the EOT marker, the data will be written but a Tape Status Alert (TSA) termination will occur. EOT will remain set until passed in the reverse direction.

If a Write Data command is issued while the tape is positioned at BOT, the PE identification burst (IDB) will be written onto the tape. This should clear the Density Check (DCK) status bit if it was set. If DCK did not clear, the transport is faulty. If any Write command is issued with the DCK bit set and the tape not positioned at BOT, no data will be written and Tape Position Lost termination will occur. If a Write Retry command is issued while the tape is positioned at BOT, a Function Reject termination will occur, with the Nonexecutable Function (NEF) error bit set in XSTØ.

During Writes, the controller generates a parity bit for each data byte sent to the transport; the transport then writes this bit along with the data byte onto tape. During the write, the transport also reads the written bytes from tape and checks the parity; the data is also sent to the controller, which also checks the parity. Therefore, two types of data errors can arise during a write: a correctable error or an uncorrectable error. In either case, the CPU should immediately issue a Write Retry command to rewrite the data correctly.

3.3.4.6 Position Command -- Figure 3-24 illustrates the Position command packet. This command causes tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to BOT. The tape-mark/record count is the second word of the command packet. This word is ignored for a Rewind command.

The allowable Mode field codes and their functions are:

Mode	Function
ØØØØ	Space Records Forward
ØØØ1	Space Records Reverse
ØØ1Ø	Skip Tape Marks Forward
ØØ11	Skip Tape Marks Reverse
Ø1ØØ	Rewind (Record Count Ignored)

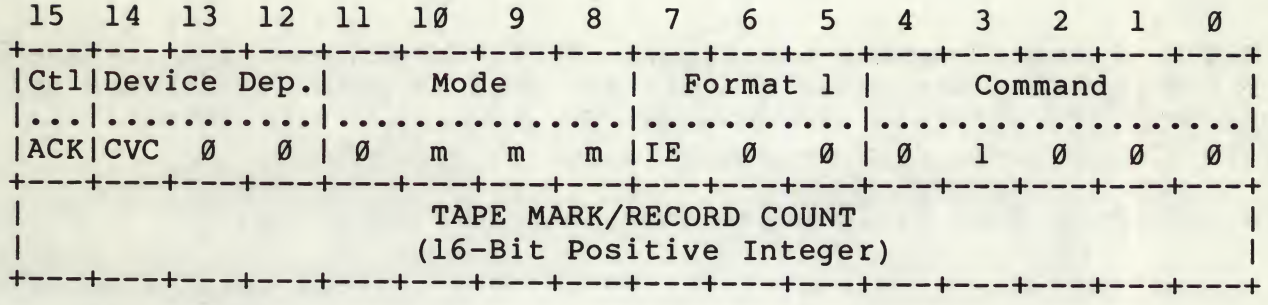


Figure 3-24 Position Command Packet

The Space Records operation skips over the number of records specified in the Record Count word of the command packet. However, the operation automatically terminates, with a Tape Status Alert termination code, when a tape mark is traversed. (The Tape Mark is included in the record count.) Also, the Record Length Short (RLS) status bit in XSTØ will be set if the record count is not decremented to zero.

A Skip Tape Marks command will skip over the number of tape marks specified in the Tape Mark Count word of the command packet. However, the operation will be automatically terminated if a double tape mark (two contiguous tape marks without intervening data) are encountered and the Enable Skip Stop (ESS) bit was set in the Characteristic Mode word on the last Write Characteristics command. Termination will also occur if a tape mark is the first record off of BOT and ESS and ENB bits are set in the Characteristic Mode word. Record Length Short (RLS) is set if the Tape Mark count is not decremented to zero.

A Space Records Reverse or Skip Tape Marks Reverse which runs into BOT sets the Reverse Into BOT (RIB) status bit and causes a Tape Status Alert Termination. If one of these reverse commands is issued while the tape is already positioned at BOT, the Nonexecutable Function (NEF) error bit will be set and Function Reject termination given; in this case, the tape will not move. If the Density Check (DCK) error is present when a Position command is issued, the DCK bit is set, but the operation is not stopped. It will terminate with Tape Status Alert. This allows tapes with a bad IDB area to be read.

When a Rewind command is issued, the interrupt (if enabled) will not occur until the tape reaches BOT and has stopped.

3.3.4.7 Format Command -- Figure 3-25 illustrates the Format command packet. Note that the second word is present (fetched by the controller) but is not used in the command. This command can write a tape mark, rewrite a tape mark, or erase tape.

The allowable Mode field codes and their functions are:

Mode	Function
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)

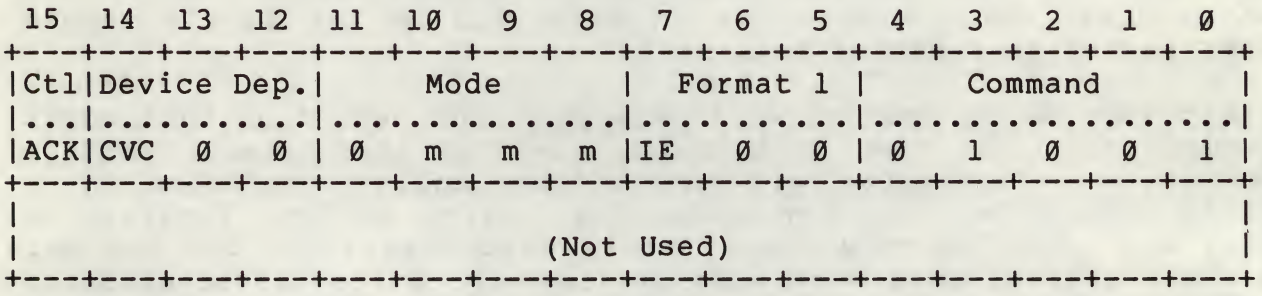


Figure 3-25 Format Command Packet

In all cases, executing a Format command at or beyond EOT will cause a Tape Status Alert termination. The EOT bit will remain set until the EOT marker is passed in the reverse direction.

A Write Tape Mark or Erase command issued at BOT will automatically cause the PE Identification Burst (IDB) to be written on the tape. If, during this operation, the IDB is not received from the transport (i.e., there is a transport or cable problem), the Density Check (DCK) error will be set and Tape Position Lost termination will occur.

If the Density Check bit is already set and the tape is not at BOT, a Format command will be aborted with Tape Position Lost termination; the tape will not move.

The Write Tape Mark command causes approximately 3.75 inches of tape to be erased and a file mark to be written. The Erase command merely causes 3.75 inches of tape to be erased. Successive Erase commands can be used to erase more than 3.75 inches (3.75-inch increments).

The Write Tape Mark Retry command causes a space reverse (over the previous record), followed by an erase of 3.75 inches of tape, followed by a Write Tape Mark (which erases 3.75 more inches of tape before writing the file mark). If the tape is positioned at BOT when the Write Tape Mark Retry command is issued, the operation will be aborted with Function Reject termination and the Nonexecutable Function (NEF) error bit will be set.

3.3.4.8 Control Command -- Figure 3-26 illustrates the Control command packet. The are three normal modes (Message Buffer Release, Rewind and Unload, and NO-OP) and one additional mode, (Rewind with Immediate Interrupt). The Control command is characterized by the fact that termination (and an interrupt if the IE bit is set) occurs immediately at the start of the command.

The allowable Mode field codes and their functions are:

Mode	Function
0000	Message Buffer Release
0001	Rewind and Unload
0010	NO-OP (Performs Clean Tape function in TS11)
0100	Rewind with Immediate Interrupt

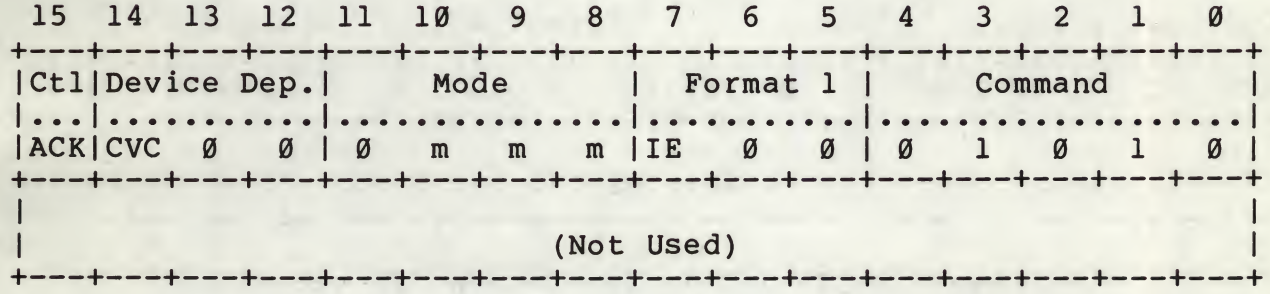


Figure 3-26 Control Command Packet

The Message Buffer Release command, when executed with the ACK bit set, allows the controller to own the Message Buffer so it can update the status in the message buffer area on an Attention (ATTN). This would be used when the CPU is not operating the TSV05 for a period of time but desires to be notified of a change in status or a microdiagnostic error.

The Rewind and Unload command rewinds the tape completely onto the supply reel and places the transport in the Off-Line state. When this command is executed, termination (and an interrupt if IE is set) will occur immediately.

When the NO-OP command is issued, normal termination will occur immediately and no tape motion will result.

The Rewind with Immediate Interrupt command causes the tape to be rewound to BOT. This command differs from the normal Rewind command in that termination response to the CPU occurs at the start of the rewind rather than when the tape reaches BOT. This command would therefore be used in a multi-transport system when it is desired to select another unit after issuing a rewind. If a transport is rewinding and another tape motion command is issued to it, the new controller will wait until the tape has been rewound to BOT before proceeding with the new command. During execution of a Rewind with Immediate Interrupt, the Motion (MOT) bit in XSTØ will be set if a Get Status command is performed.

3.3.4.9 **Initialize Command** -- Figure 3-27 illustrates the Initialize command packet. If there are no microdiagnostic errors, this command is treated as a NO-OP. If there are errors present, however, the command performs the same as a write into the TSSR register. In either case, IFEN to the Tape Transport is pulsed to stop runaway commands.

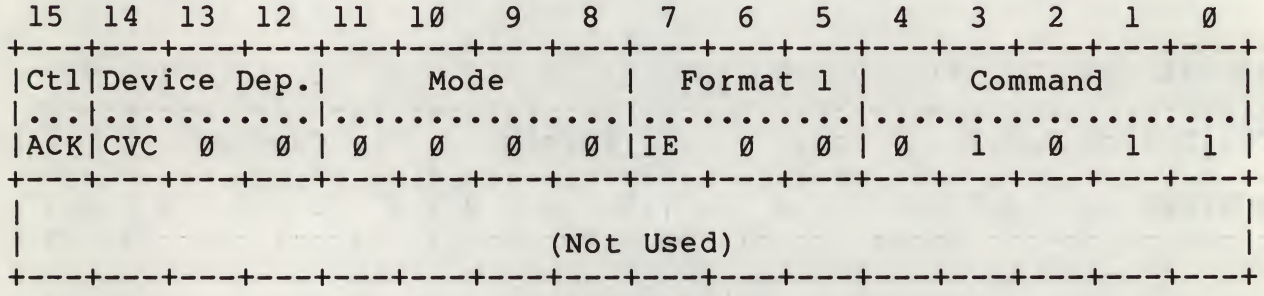


Figure 3-27 Initialize Command Packet

3.3.4.10 **Write Subsystem Memory Command** -- This command is used for the diagnostic programs, and is not applicable to programming for normal operations.

3.3.5 Record Buffering

The Record Buffering mode of operation can be invoked to optimize system performance when performing Read and Write operations on a "streaming" tape transport. The technique causes tape records to be "cached" (buffered) in the controller in order to avoid many of the long repositioning delays frequently encountered when dealing with a streaming tape transport. Repositioning occurs if the transport does not receive its next command before the reinstruct period expires. On a typical system, the chances are high that, in a non-buffering mode, the software will miss the reinstruct period (e.g., data to be written must be transferred from a disk, or data read must be transferred to a disk, etc.) since the software cannot always keep the transport busy. Buffering is a means to decrease the number of repositionings while transferring a file of sequential records. The effect of buffering serves to lengthen the apparent reinstruct period (as seen from the CPU) since tape data transfers can be overlapped with the CPU operations required to prepare for issuing the next command to the tape subsystem.

Read buffering causes an additional record to be read from tape in response to a program requesting just one. Typically, a program requests several records in succession, so a record stored in the controller will be available for immediate transfer to the CPU and can be transferred while another record is being read or the tape is repositioning. Only the Read Next command (e.g., a forward read) causes the buffering algorithm to be invoked.

Write buffering allows one record to be accumulated within the controller and subsequently written to tape, allowing transfer of data from CPU memory to controller to be overlapped with tape repositioning. This also allows the CPU to prepare and issue the next Write command while the previous (stored) record is being written to tape. Therefore, there can be two records ready for transfer. One in the controller and one in CPU memory.

Record Buffering is enabled either by software or hardware. If the Extended Features switch is set, it can be enabled or disabled via the "extra" (5th) Characteristics Data word. If Extended Features is off, it is enabled or disabled only by the Buffering Enable switch. The following paragraphs describe the operations performed for Read and Write buffering.

3.3.5.1 Read Buffering -- Assuming that the transport is ready for an operation (On-Line, etc.), the following occurs when a Read Next (Forward) command is issued to the controller and buffering is enabled:

1. When a Read Next command is issued, the tape is started and data is transferred from tape to CPU memory in the normal fashion.

2. When the final byte of data from the tape has been transferred to CPU memory and the transport has negated the DATA BUSY signal, the controller tests the Status inputs from the Transport Bus and determines if any errors or special incidents occurred.

3. If an error occurred, or if a Tape Mark was read, or if the tape is beyond the EOT marker, the controller will terminate the operation by issuing the appropriate status message and will not automatically issue another command to the transport. The controller will return to its Idle state (before Step 1) and the transport will be allowed to complete its sequence.

4. If the transfer completed without incident, the controller will issue its normal Successful termination message. The program in the CPU can then act on this message (i.e., begin transfer of the data to disk, etc.).

5. If the transfer completed without incident, and if the record just read was 3.5K bytes or less in length (e.g., could fit entirely within the controller's RAM), the controller will issue another Read Forward command to the transport and read the next record from tape and store the data in its internal RAM (up to 3.5K bytes of data). This operation can be termed "pre-reading".

6. When the next record has been read, or if an "incident" occurs (Tape Mark, EOT, or error), whichever occurs first, the tape drive will be allowed to stop. In addition, if, during a pre-read, data on tape is not encountered within 1 second, the pre-read will be aborted and the tape allowed to stop, since there may be no more data on the tape; if this is the case and a Read Next is eventually issued for this nonexistent record, the operation will terminate with an OPI error after 25 feet of tape have been passed without encountering data.

7. While the controller is pre-reading the next record, it is monitoring the LSI-11 Bus Interface for the next command from the CPU.

8. If the next command is Read Next, the controller immediately begins transferring the pre-read data record from RAM to CPU memory (this transfer can be performed during the pre-read of data from tape).

9. When the pre-read record has been transferred entirely to CPU memory, the controller issues another Read command to the transport and the cycle repeats.

10. If additional sequential Read Next commands are issued, data is supplied from the RAM until its contents are exhausted. The cycle then repeats from Step 1 if another Read Next is issued.

11. If an End of File mark is encountered on tape, or if any errors occur, pre-reading of records ceases. If errors occur, the controller spaces one record reverse (only if the 25-foot timer did not abort on the pre-read.) The tape will be logically positioned just before the record of incident. If and when a Read command is received from the CPU to read a record, normal read operation will occur. If the 25-foot timer expired from the previous pre-read, Tape Position Lost will be reported in response to this read command. If an End of File mark is encountered on tape, the controller records this, and does not move the tape. The next command handles the File Mark appropriately.

12. If any command other than a Read Next is issued by the CPU, and if the controller RAM still contains a pre-read record, the new command is stored internally (so that action may eventually be taken) and the controller performs a recovery action as follows:

    a. If a record is currently being read from tape, the controller allows the operation to complete and the transport to negate Data Busy.

    b. If the new command is a Space Records (either forward or reverse), the current tape position is compared with the tape position assumed by the CPU program (based upon the last record transferred to CPU memory). The controller recomputes the recordcount required to reach the final target position and enters the normal Space Forward or Space Reverse sequence, using the new record count.

    c. If the new command is a Rewind or Rewind/Unload, the rewind sequence is immediately performed; no further adjustment in tape position is required.

    d. If the new command is a Skip Tape Marks, the controller determines if it contains an outstanding pre-read file mark and recomputes the skip count. If there is no pre-read file mark, no adjustment is necessary. If one exists, the count as supplied by the CPU is adjusted by one (plus or minus). The normal skip sequence is then entered.

e. If the new command is other than those listed above, the controller repositions the tape by skipping one record in reverse (to space back over the pre-read record outstanding) before executing the new command.

13. If, during pre-reading, data from the current tape record will not fit into the space currently available in RAM, the tape operation is aborted and the controller directs the transport to space reverse in order to recover proper tape position. The controller does not attempt to pre-read the record that was aborted.

3.3.5.2 Write Buffering -- Record Write Buffering allows the CPU to issue successive Write Data commands to the controller, with the controller storing one record up to 3.5K bytes in length in its RAM. When a Write Data command is first received, a "fetch from memory" process is started to transfer data from CPU memory to the controller RAM. Then, when at least one byte of data is available in RAM, the tape transport is directed to write and an "output to tape" process is started to transfer data from the RAM to the FIFO. These processes are relatively independent, with a supervisory loop overlayed to keep track of RAM buffer management and abnormal conditions.

Initially, the tape is probably at rest or in a repositioning cycle. Therefore, the "access time" (the time elapsed since the controller commanded the transport to write, and the time when the first character was strobed out of the FIFO and written onto tape), is relatively long. During this time, another Write Data command can be accepted from the CPU (but not given a termination response), with the associated data held in CPU memory. When in buffering mode, a Successful termination status is given to the CPU as soon as a record has been transferred completely from CPU memory to RAM, thereby allowing the CPU to issue another Write Next command. It is therefore possible that the "output to tape" process is one record behind the "accept new command" process. The overall effect is to allow the CPU to overlap the preparation of one record with the writing to tape of the previous record, allowing the controller to command the transport to write within its reinstruct time.

If a record is specified to be greater than 3.5K bytes (the amount of RAM allocated for buffering), the record is handled in the non-buffered mode: termination status is not given to the CPU until the record has been written entirely onto the tape or an error occurs.

When writing a record that is not associated with the current command (last issued by the CPU), the controller performs an automatic error recovery (retry) procedure (space reverse, erase, then write forward) up to 1Ø times. Hence the necessity for a record to reside completely within the RAM when buffering. If the Extended Features switch on the M7196 is set, the extra (5th) Characteristics Data word can specify the number of retries (from Ø up to 15) and can specify that a long gap should not be generated on an automatic retry (the Erase function is eliminated from the recovery sequence).

During the Write Buffering mode of operation, the controller reads a block of data into its RAM from CPU memory then responds to the CPU with a normal successful completion status. As far as the CPU software is concerned, then, the record was written on tape successfully. The controller must therefore take all the steps possible to eventually write that record onto the tape. Hence the need automatic retries. Write buffering is a more complex operation than Read buffering because of these retries. Furthermore, should the worst occur and the controller cannot write a buffered record, the CPU program will not know exactly which record failed to be written (the program could conceivably believe that a record was written properly when in fact it was not). For this reason, a Tape Position Lost error termination is given for the next Tape Motion command issued by the CPU if a buffered record cannot be successfully written. In addition, if a buffered record is successfully written after retries, the CPU will have no way of logging the fact that some trouble was encountered.

Because of the potential difficulties described above, the controller implements an adaptive buffering algorithm. In this algorithm, the first Write Data command following any type of command other than a Write Next or Write File Mark is handled in a non-buffered mode: termination status is not returned to the CPU until the actual write-to-tape operation is complete. If the record was written without error, then subsequent Write Data commands will cause buffering of the data. If an error occurred on this first record, the CPU can take its normal error logging and recovery procedures. Buffering will not be enabled again until a successful record is written without retries.

Assuming that the transport is write-enabled and ready for an operation, the following occurs when a Write Data command is issued by the CPU and buffering is enabled (but not currently activated by having just completed a successful Write Data or Write Tape Mark):

1. When the Write is received by the TSVØ5, the controller issues a Write Command to the Tape Transport, and begins transferring the associated data from CPU memory to RAM.

2. As soon as the first word appears in RAM, it is transferred to the FIFO.

3. The previously issued Write command to the transport will eventually begin emptying the FIFO and writing the data onto tape.

4. Meanwhile, the transfer from CPU memory to RAM continues as long as there is room in the RAM; the transfer from RAM to FIFO continues as long as there is room in the FIFO.

5. Since this is the first Write, it is being handled in a non-buffered mode so the "memory to RAM" process is allowed to overwrite a RAM byte that has already been transferred to the FIFO. The RAM management algorithm has the capability of suspending transfers either into or out of the RAM so that bytes not already transferred to the FIFO do not get overwritten, and so that the FIFO receives only valid bytes. (The RAM is handled as a circular buffer.)

6. When the final byte of data associated with this command has been written onto the tape and the transport has negated DATA BUSY, the controller tests the Status inputs from the transport bus and also its internal status (i.e., FIFO overrun) for errors or exceptional conditions.

7. If an error occurred or EOT was seen, the controller will terminate the operation by issuing the appropriate status message and will not enable itself for write buffering. The controller reverts to its Idle state (before Step 1) with buffering deactivated.

8. If the transfer completed without incident, a normal successful termination message will be issued and the controller will enable itself for buffering of future Write commands.

9. If the next command is indeed a Write Data, operation proceeds as in Steps 1 through 4 above. However, when all the required data has been transferred from CPU memory to RAM, and if the record will fit entirely in RAM, and if no exceptional condition has yet occurred, the controller will issue normal successful termination status to the CPU. As far as the CPU is concerned, the record has been written onto the tape, although this is not really the case.

10. The controller continues transferring data from RAM to FIFO until the record it is currently transferring has been completely written onto tape. If the transfer is successful, the record is purged from the RAM, freeing its space for another record from the CPU. In addition, if no incident has occurred with the transfer, the controller will accept another Write Data command from the CPU and begin transferring data into the RAM.

11. As long as no errors are encountered, another Write command will continue to be accepted and the three previous steps repeated.

12. If an error occurs, the controller enters its retry algorithm to attempt to successfully write the current record (space reverse, possibly erase forward, and rewrite the record using data stored in RAM). Statistics are kept as to the number of retries completed. If, after the specified number of retries (10 is the default), the record cannot be successfully written, operation is aborted and an error message (Tape Position Lost) is issued to the CPU (if possible) as follows:

    a. Tape Position Lost status will be issued on the next motion type command received by the controller.

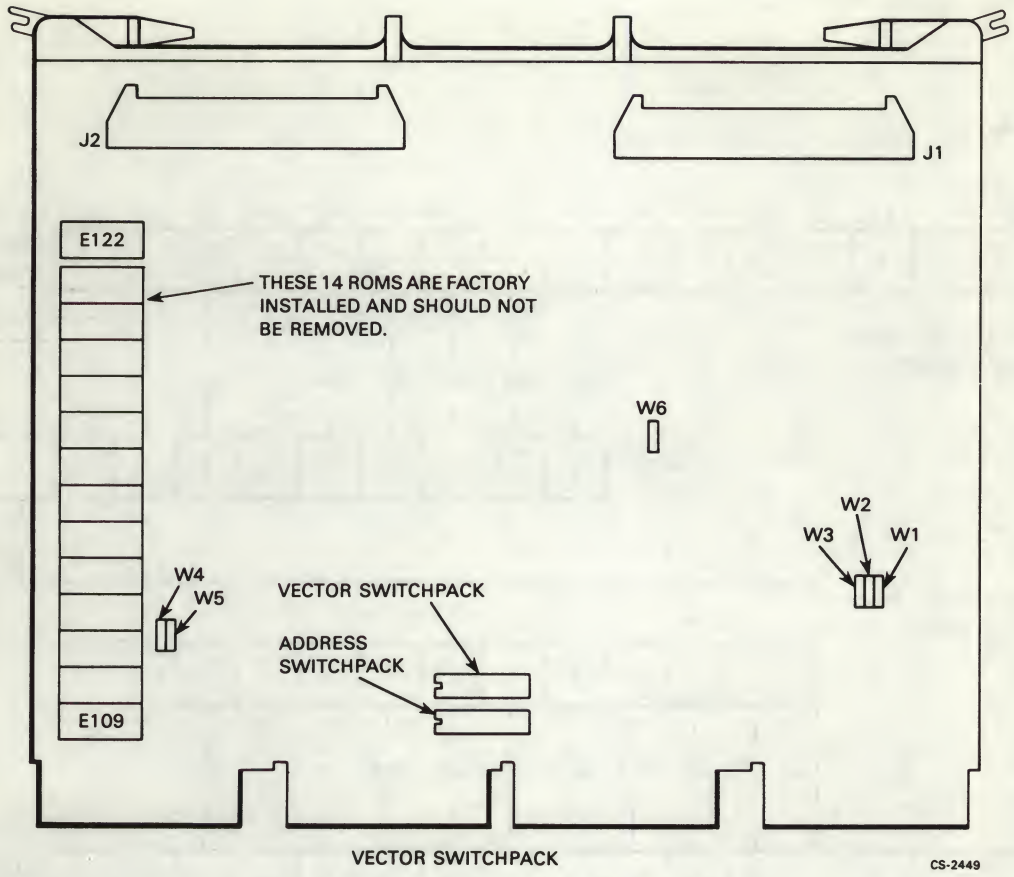
13. Assume an error occurs and the record can be successfully written within the retry constraints. If a Write command was currently pending (termination status not yet issued to the CPU) when the recoverable error occurred, it is then allowed to complete in the normal unbuffered fashion (so the CPU can log any errors). If this record is successfully written, buffering will again be enabled and will wait for the next command at Step 9. If the record required retries by the CPU, the controller will then return to its Idle mode (before Step 1), causing the next Write command to be handled in the unbuffered mode.

14. If, during the normal sequence of processing sequential Write commands, buffering the records, and writing them to tape, a Tape Motion command other than Write Data is encountered, the RAM is purged (a stored record written to tape) before the new command is processed. Write Buffering is disabled until a successful Write Command. Therefore, after this new command is processed and its termination status issued, the tape is positioned as expected by the user and all outstanding conditions reconciled.

15. Similarly, if a Write Next command specifying a record larger than 3.5K bytes is processed, this command will be handled in the unbuffered fashion, but will allow buffering to be attempted if the very next command is Write Next.

NOTE

Initialization (Bus INIT or a write into TSSR) should be avoided, since it purges the RAM and current status. When this is done, it is possible to lose a record that the user might asume was properly written.



VECTOR SWITCHPACK

	1	2	3	4	5	6	7	8	9	10	
ON / OFF	V8	V7	V6	V5	V4	V3	V2	S1	S0	A12	E58

ADDRESS SWITCHPACK

	1	2	3	4	5	6	7	8	9	10	
ON / OFF	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	E57

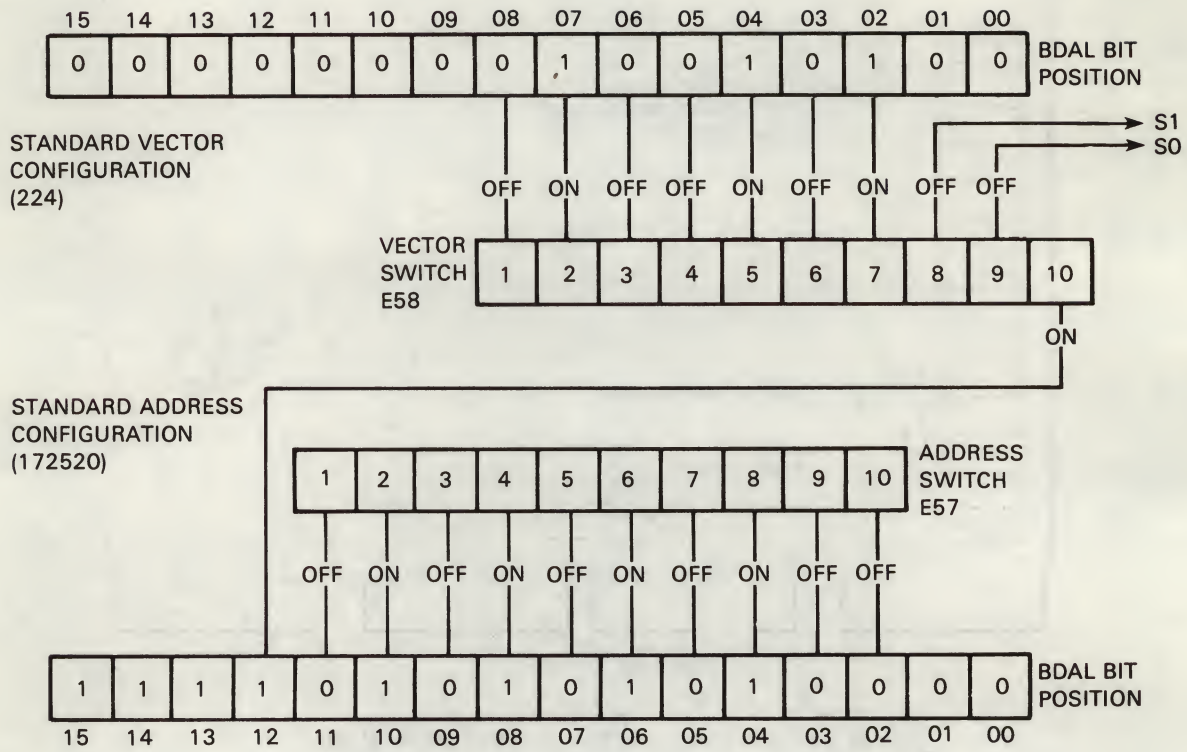
V = VECTOR BIT
A = ADDRESS BIT
S1 = BUFFERING
S0 = EXTENDED FEATURES

JUMPERS		AS SHIPPED
W1	BIRQ5	OUT
W2	BIRQ7	OUT
W3	BIRQ6	OUT
W4	BUS GRANT CONTINUITY	IN
W5	BUS GRANT CONTINUITY	IN
W6	SCLOCK ENABLE (USED DURING FACTORY REPAIR ONLY)	IN

CS-2450

Figure A-1 M7196 Switch and Jumper Identification

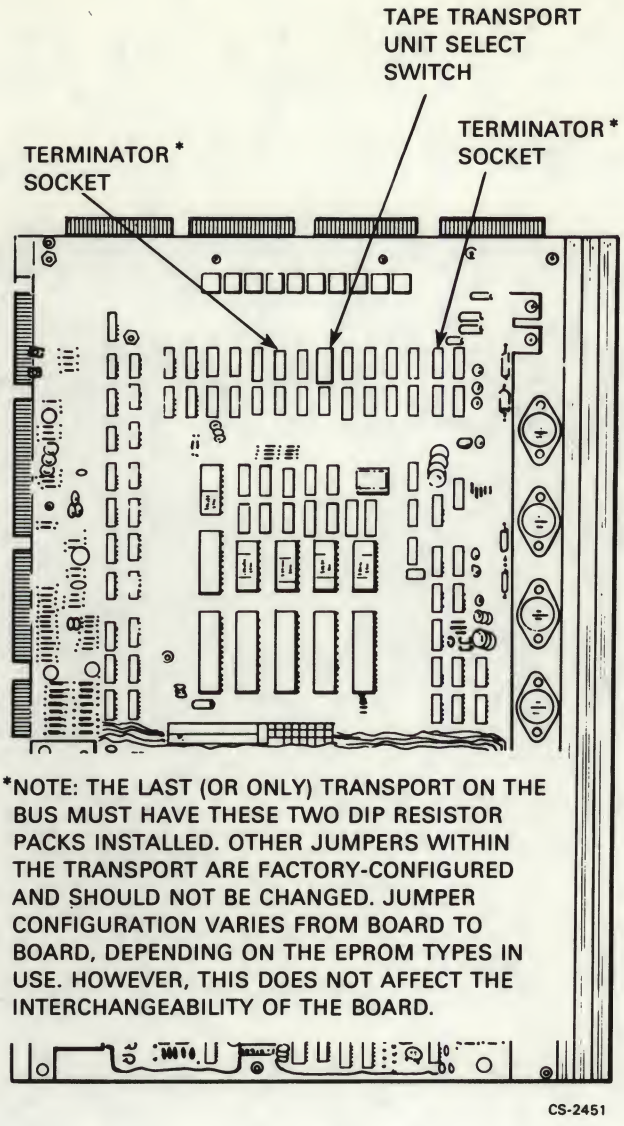
M7196 VECTOR AND ADDRESS SWITCHES



SO = EXTENDED FEATURES
S1 = BUFFERING

CS-2468

Figure A-2 M7196 Vector and Address Switches



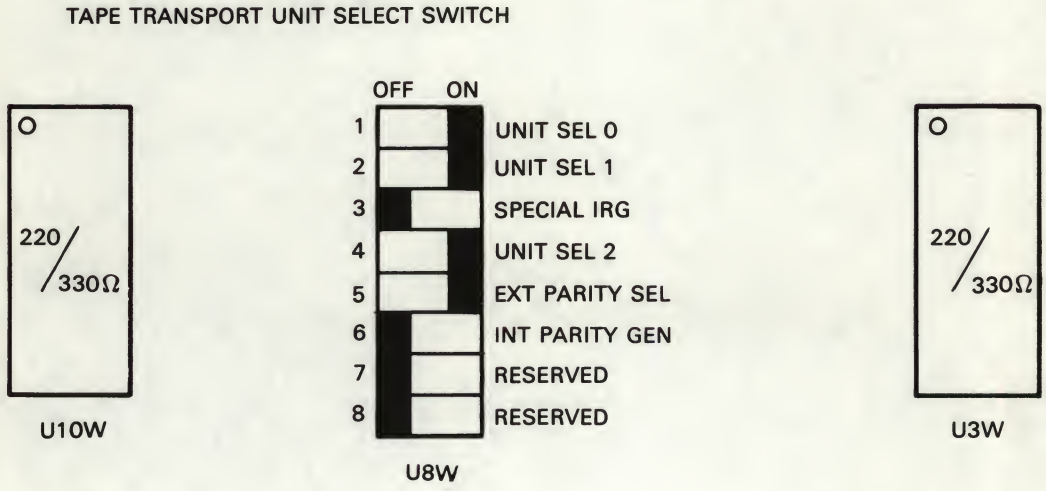


Figure A-3 Transport Switch and Terminator Identification

APPENDIX B
MANUAL LOADING

If the autoloading routine does not successfully load the tape, the manual loading procedure may be used. Refer to Figure B-1 and proceed as follows:

1. Switch off the tape transport power.

2. Raise the cabinet top cover by grasping the handle on the top cover and lifting. When the top cover is raised far enough, the support arm latches to keep the cover up.

3. Raise the top cover of the tape transport unit by reaching in through the front panel door and pushing upward on the front of the top cover.

4. Ensure that there are no foreign objects in the tape path.

5. Place the reel of tape on the supply hub. Ensure that it is evenly seated on the hub, and then close the front door.

6. Thread the tape along the tape path as shown in Figure B-2. Carefully move the tachometer assembly away from the takeup hub and wrap the tape clockwise around the hub. Wrap the tape just short of one complete turn. Note that the tape should not overwind at this point (i.e., there should be a short section of the takeup hub that has no tape on it yet).

7. Gently move the tachometer assembly back against the hub. (The tape should pass between the tachometer and the takeup hub.)

8. Check that the tape is seated correctly on the guides and threaded properly over the head assembly. Remove any excess slack by gently turning the supply reel counterclockwise.

9. Turn the takeup hub clockwise to wrap two additional turns of tape on the hub. Ensure that the tape does not ride up and extend over the top surface of the hub.

10. Close the top covers of the tape transport and the cabinet.

11. Switch on the tape transport power.

12. Press ENTER, with ENTER depressed, press LOAD. When the LOAD indicator stops blinking, the tape is loaded and ready to be switched on-line.

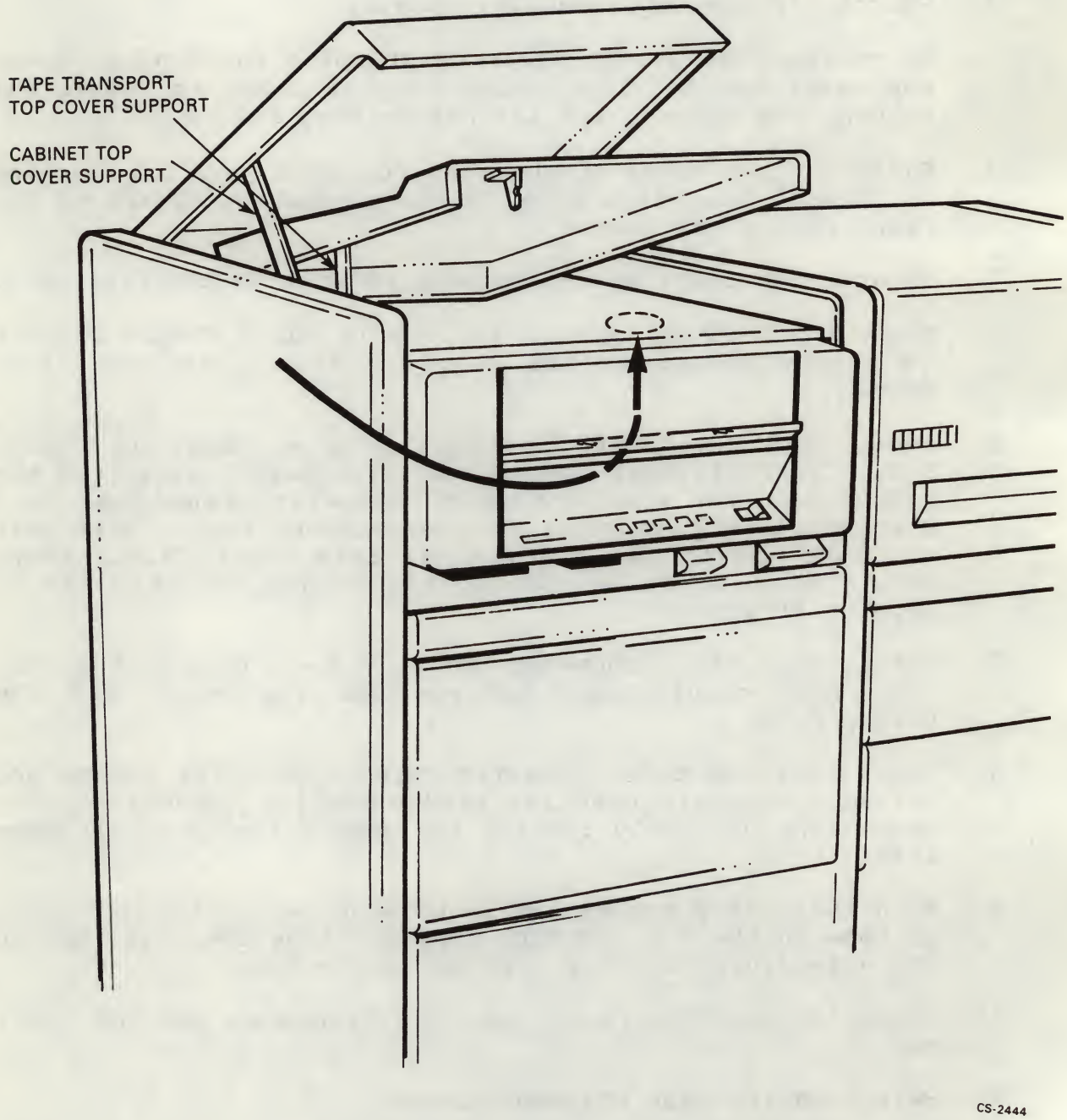


Figure B-1 Accessing the Tape Path Area

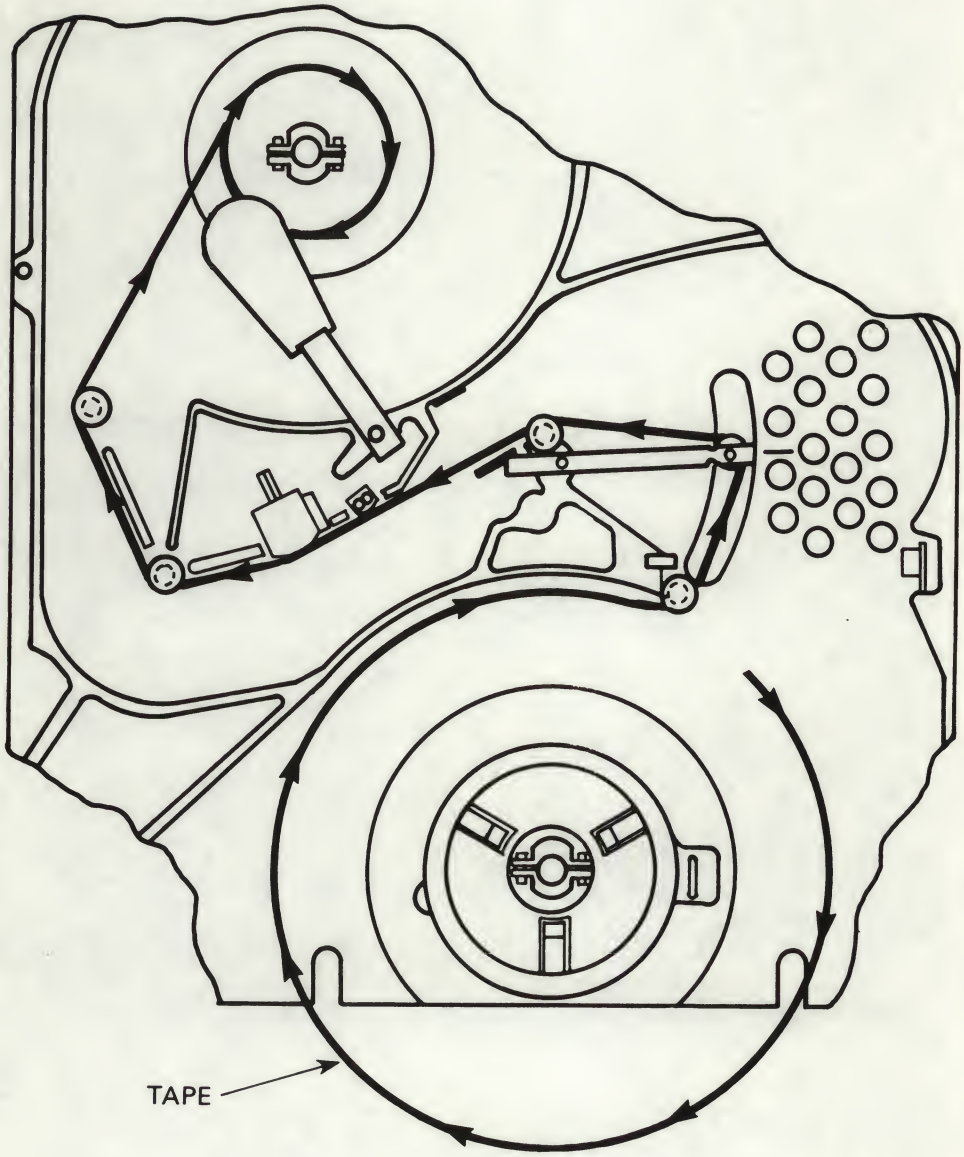


Figure B-2 Tape Threading Path

APPENDIX C
SUMMARY OF KNOWN DIFFERENCES

The following list describes the known programming differences between the TS11/TSØ4 Magtape Subsystem and the TSVØ5 Magtape Subsystem, with the TSVØ5 in "TS11 Compatibility" mode (Extended Features switch off and record buffering disabled).

1. In the TSVØ5, control logic resides in the M7196 Controller/Interface module (allowing non-tape-motion commands to be executed with the transport power off), whereas in the TS11, control logic resides in the tape drive (preventing any commands from being executed with tape drive power off).

2. TSDB/TSBA Data Wraparound Maintenance Functions: The TSVØ5 uses (wraps around into the TSBA) only the byte that was written into TSBD, whereas the RS11 wraps around both bytes from the bus (the contents of the byte not specifically written is not always known, since it varies with CPU type). In addition, a word-write maintenance function is defined for TSBD that is not available in the TS11.

3. TSSR Register: Bit 14 and 13 have differing meanings between the two subsystems. On the TS-11, bit 14 indicates a Unibus Parity Error (UPE), while in the TSVØ5 it is not used. On the TS11, bit 13 indicates Serial Bus Parity Error (SPE), while on the TSVØ5 it indicates a Sanity Check Error (SCE), an error detected by the controller in its RAM while performing Micro Diagnostics.

4. TSSR Register: In the TSVØ5, this register is also used to indicate self-test errors detected upon initialization.

5. Extended Status Register 1 (XST1): Bits 12-9, 7-2 and Ø are not used by the TSVØ5 and always appear as Ø, while in the TS11 these bits detail the cause certain errors on a tape motion command. This detail is not presently available from the TSØ5 tape transport used in the TSVØ5 subsytem.

6. Extended Status Register 1 (XST1): Bit 8 is not used on the TS11, while on the TSVØ5 it indicates a parity error detected on the Read Data lines from the transport.

7. Extended Status Register 2 (XST2): Bit 14 on the TS11 indicates I/O Silo Parity error (SIP), while on the TSVØ5 it indicates a RAM Checksum Error (RCE).

8. Extended Status Register 2 (XST2): Bits 13, 12, and 8 are not used on the TSVØ5, while on the TS11 these bits indicate Serial Bus Parity Error at Drive (BPE), Capstan Acceleration Fail (CAF), and Dead Track Parity (DTP).

9. Extended Status Register 2 (XST2): Bits 7-Ø, on a tape motion command, on the TS11 indicate tracks which when dead, while on the TSVØ5 this information is not available from the TSØ5 transport.

1Ø. Extended Status Register 2 (XST2): Bits 7-Ø, on a write Characteristics command, indicate the microcode revision level on both machines. In addition, the TSVØ5 indicates the settings of the extended features enable switch (bit 7) and the buffering enable switch (bit 6). On commands other than write characteristics the TSVØ5 displays the unit number of the currently selected transport in bits 2-Ø.

11. Extended Status Register 2 (XST2): Bits 7-Ø, on a Get Status command, on the TS11 indicate the "residual capstan tick count, while on the TSVØ5 this information is not available from the TSØ5 transport.

12. Extended Status Register 3 (XST3): Bit 7 is not used on the TSVØ5, while on the TS11 it indicates Tension Arm Limit Exceeded (LMX).

13. Extended Status Register 3 (XST3): Bit 4 on the TS11 is to report Capstan Response Failure (CRF), while on the TSVØ5 it is not used.

14. Extended Status Register 3 (XST3): Bits 2 and 1 are not used on the TSVØ5, while on the TS11 these are used to indicate a Noise Record (NOI) and Limit Exceeded Statically (LXS), respectively.

15. The Clean Tape is handled as a NO-OP in the TSVØ5; tape does not move.

16. The Write Subsystem Memory Command is entirely different between two machines.

17. Tape speeds, and therefore data transfer rates, differ: 45 ips for the TS11, and 25 ips for the TSVØ5.

18. Data access characteristics differ, since TS11 uses a Stop/Start tape drive and TSVØ5 uses a Reel-to-Reel (Streaming) tape drive.

TSV05 TAPE TRANSPORT SUBSYSTEM USER'S GUIDE
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